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DIGITAL EXECUTIVE CONTROL OF A HYBRID COMPUTING SYSTEM

by

Glenn E. Kauffman

A Thesis Submitted

in

Partial Fulfillment

of the

Requirements for the Degree of

MASTER OF SCIENCE

in

Electrical Engineering

Approved by:

Prof. George A. Brown
(Thesis Advisor)

Prof. George Thompson

Prof. Robert E. Lee

Prof. W. F. Walker
(Department Head)

DEPARTMENT OF ELECTRICAL ENGINEERING
COLLEGE OF ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY
ROCHESTER, NEW YORK
JUNE, 1972

ABSTRACT

This is a paper describing an interface system integrating an HP 2116B digital computer and an EAI TR-48 analog computer. The interface system provides the digital computer with the capability to control the analog computer operational modes, to read the output signals on the analog computer amplifiers and coefficient settings of the potentiometers, and to control and sense numerous interface trunks.

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I. INTRODUCTION

This thesis is the description of an Interface System that was designed and built for the Rochester Institute of Technology (RIT) Electrical Engineering Department Hybrid Computer Laboratory in partial fulfillment of the requirements for the Master of Science Degree in Electrical Engineering.

The thesis entails all aspects of systems concepts, requirements and definition of an Interface for the Electrical Engineering Department's Hewlett-Packard (HP) 2116B digital computing system, Electronic Associates Incorporated (EAI) TR-48 analog computer and EAI Digital Expansion System (DES-30). The project has been to define, design, develop, fabricate, test, and document a viable digital and analog interface to accomplish mode control of the analog computer by the digital computer, and addressing and reading the analog computer amplifiers (amps) and potentiometers (pots, also called attenuators) from the digital computer. Problems associated with this project have been timing, switching, buffering, and voltage level conversion to make the digital computer, analog computer, and digital expansion system compatible. Special regard has been given to human factoring for ease of system operation, simplicity of design, modularity, and construction economy while maintaining flexibility and accomplishing the tasks required for hybrid computer problem solving by faculty and students at the Rochester Institute of Technology (RIT).

Numerous other attempts at Hybrid Computers have been studied in order to gain ideas of types of hybrid systems and problems being solved on these systems. However, the equipment available and the envisioned usage has necessitated a tailored system for RIT's purposes.

The tailored Interface system described in detail herein provides the following capabilities:

I. The interface controls the modes of the analog computer, and DES-30 from the user's FORTRAN or Assembly Language program on the digital computer.

   A. The modes available on the TR-48 are

      1. Operate
      2. Reset (Initial Conditions)
      3. Hold
      4. Pot Set
      5. Time Scale Fast/Normal

   B. The modes available on the DES-30 are

      1. Run
      2. Clear
      3. Stop

II. The interface addresses the analog computer amplifiers and potentiometers from the user's FORTRAN or Assembly Language program. The value of the addressed amplifier or potentiometer is listed on the Teletype associated with the digital computer.

III. The interface addresses a number of digital control trunks terminating on the patch panel of the DES-30. These digital control trunks may be patched on the DES-30 and/or through the DES-30 D/A trunks to the TR-48 for a

variety of logical functions such as function generation, counting, limiting, tracking, and storing. The control of these lines is achieved through the user's FORTRAN or Assembly language program on the digital computer and is dictated by the specific hybrid problem being solved.

IV. The interface senses a number of digital sense lines originating on the patch panel of the DES-30. These digital sense lines may be patched from the DES-30 and/or from the TR-48 through the A/D trunks for a variety of logical functions and may be used in conjunction with the digital control lines, digital mode control, and amplifier and potentiometer readout.

More detail of these capabilities may be found in later sections.

A manual ANALOG/HYBRID Master Switch has been provided to connect the analog computer, digital computer, and digital expansion system into an integral system when in the HYBRID position, and to divorce the functions required to make the units three separate entities for use individually when in the ANALOG position.

Other sections of this report describe the evolution of the current operating system, hardware and software details, user's instructions, changes to manuals, actual performance parameters, recommendations,

and original objectives -- how and to what extent they were accomplished, and conclusions.

II. OBJECTIVES

The original objectives of this thesis were to build an operable interface 1) for the purpose of mode control of the analog computer from the digital computer and, 2) for the purpose of listing the values of the analog amplifiers (amps) and potentiometers (pots) on the teletype unit preceeding or succeeding the solution of an analog problem.

Furthermore, any software was to have been written in Assembler Language to conserve the amount of computer memory required to store the software programs. The interface software was to provide the capability of reading one pot or amp for each time it is called from the hybrid computer user's controlling program with the pot number or amp number specified by the user's program. The interface software was to have the capability of being called serially in rapid succession by the user's program for multiple listings. The listing of potentiometers and amplifiers was required only in periods when the analog solution is not in progress, the theory being that the voltages on amplifiers may be read much faster during an analog solution by the digital computer using the Analog-to-Digital (A/D) converter provided on the digital computer by patching the selected pot or amp on the analog computer patch panel to the appropriate A/D converter trunk termination.

Since the TR-48 analog computer does not contain servo

set potentiometers, there has been no requirement for the interface system to set potentiometers in a dynamic, closed-loop fashion.

As the funds for building an interface system were very limited, the scheme for the interface system was required to produce a viable system at low cost. The original estimate made to the Electrical Engineering Department for the cost of materials for this project was $400-$1000, with the stipulation that minimal expenditure would be made until feasibility had been proven through experimentation and breadboarding.

For economic reasons, as well as human factors, reliability and maintenance, the system was to be designed as simply as possible to achieve the aforementioned tasks, as well as maintaining flexibility for the user and capability for further additions.

All the original objectives have been accomplished in this thesis.

III. REVIEW OF LITERATURE

A. History

About four hundred years ago one of the first analog computers, the slide rule, was invented.

During the second World War, mechanical analog computers, known as differential analyzers, were widely used.[16]

Since then, the advent of the electronic analog computer, the digital computer, and the analog/digital or hybrid computer has revolutionized not only mathematical analysis, but the entire space-age world.

"The hybrid computer was a marriage of necessity, born by the requirement to simulate ballistic missle systems in the late 1950's".[8] The problem of speed and accuracy consumated this marriage.

The advantages of hybridization were recognized in the early 1950's. The drawbacks at that time, however, were the use of vacuum tubes for interface elements, the lack of a digital computer for on-line operation, and the lack of adequate software.[1]

The analog computer is characterized by high solution speed (which requires high frequency or large bandwidth components), but relatively low accuracy solutions. The digital computer is characterized by high accuracy, but relatively slow speed compared to the analog machine. So, the marriage of the analog and digital computers to

form the hybrid computer is an attempt to usurp the best from both worlds.

The conception of the hybrid computer was motivated by the requirement to simulate a number of aerospace problems. Spacecraft require high performance, fast response control systems for guidance. These systems can be simulated only in real-time or faster than real-time due to the length of a mission and the need for quick updating during a mission. This is best achieved on the analog computer. However, in the spacecraft re-entry phase, errors in the entry angle of 0.1 degree or velocity of a few feet per second can result in landing errors of hundreds of miles.[8] The accuracy required here is best achieved on the digital computer. Hence, for the total system simulation, the analog and digital were joined.

The first major efforts to link the analog and digital computing systems in the late 1950's were at Ramo Wooldridge Corporation (now TRW Systems Group) in Los Angeles and Convair Astronautics in San Diego. This joining was the result of attempts to add an auto pilot and human operators to a digital simulation of missles and aircraft, and to solve three-dimensional trajectory problems associated with intercontinental ballistic missles.[1]

About 1960, Electronics Associates Incorporated (EAI) introduced an automatic digital input-output system (ADIOS)

for its analog computers. This system enabled a digital computer to set potentiometers, read components and control modes of the analog computer.[6]

A major breakthrough in the design of hybrid systems came in 1964 when Comcor/Astrodata introduced the first solid state high reliability analog computer for hybrid operation.[1] This was a giant step, for only two decades earlier one of the first digital computers (used for ballistic calculations during World War II) contained 20,000 vacuum tubes with a mean-time-to-failure of 7 1/2 minutes, weighed 30 tons, and took up the floor space of a medium-sized house.[20]

Soon after the Comcor transistorized analog system, other major analog and hybrid equipment turned completely to transistorized systems. About 1966, advanced solid state technology permitted an increase in the analog system bandwidth by about a factor of four. By this time, virtually every large company in the aerospace/aircraft industry had acquired a hybrid computing system. The advent of stand-alone dedicated, digital minicomputers drastically increased the number of hybrid computer centers. The minicomputer eliminated the need to rent and share a large digital computing system, and the minicomputer, since it was designed to be interfaced, provided simpler hardware linkages to the analog computer.

As the digital computer performance increases, more of the functions previously done by the analog machine

have been put into the digital realm. The major reasons for this are repeatability and ease of program set-up. As a consequence, the digital portion has and will continue to grow. It would logically follow that the existance of analog and hybrid computers will shortly be supplanted by the ever faster, more capable digital processors. But the analog has two characteristics which will endure. It will always be faster, and it will always be more comprehensible in the physical description of a system.

It is expected that in the 1970's the trend toward reduced dynamic range and increased bandwidth will continue in analog and hybrid machines.

"Unfortunately, no concept is being developed that unifies the analog and digital techniques into a truly hybrid computer that functions as a single entity. As it now stands, a 'hybrid' computer is the awkward connection of two separately manufactured commercial computers tied together by wires, converters and software. Computation functions gravitate to one realm or the other without much regard to the computing errors or compromises involved."[8]

Reference 19 gives detailed methods for determining the probable accuracy of an overall computer solution, given a specific hybrid configuration.

B. Reasons for Hybridization

The primary use of analog and hybrid computers is to simulate the behavior of physical systems. Simulation

enables one to study a system with all its variations, without paying to have the system built and then changing the system for parametric studies. Hybrid simulation is the modeling of complex physical systems represented by sets of differential equations, algebraic equations, and logic equations, in order to study the behavior of a system. The objectives of the simulation may be experimental design, prediction and control, design evaluation, feasibility, verification, or optimization.

Applications for hybrid computers are generally complex problems; therefore, it is best to decide the magnitude of a problem and the best means of solving the problem before blindly going to a hybrid computer for solution. Data processing system simulations are more effectively accomplished on digital computers. Electrical circuit simulation is usually more appropriately done on the analog computer. It is the simulation of total systems that brings together a combination of components, some suited for digital and some for analog simulation that hybrid computers are most beneficial. Hybrid computation offers the most economical and efficient means for solving a broad spectrum of problems which arise in many fields of science and engineering.[16]

In order to see the reasons for marrying the analog and digital computers, let's first look at the characteristics of each machine separately.

Analog Computer General Characteristics	Digital Computer General Characteristics
1. Continuous	1. Discrete
2. Parallel operation, all computing elements operate simultaneously.	2. Serial (sequential) operation.
3. Maximum accuracy about .01% of full scale, limited by the quality of components available.	3. Accuracy - bounded only by word length and amount of storage that is economically feasible for the problem solution. Accuracy is nearly independent of the quality of the components.
4. Speed - fast	4. Speed slow compared to analog.
5. Able to handle multiplication, addition, integration, and nonlinear function generations. Almost no ability to make logical decisions, store numerical data, provide extended time delays, or handle non-numerical information.	5. Able to handle multiplication and addition; more complex operations such as integration and differentiation must be performed by approximate numerical techniques.
6. Programming technique - substitutes analog computing elements having transfer functions of differential equations analogous to those of the original system.	6. Programming technique - easy programming using mneumonic instructions facilitated by language compiliers and special interpretive routines.
7. Facility for including analog hardware from a system under study in the computer simulation, also provides capability for substituting hardware subsystems into a system simulation as the subsystems are built one-by-one.	7. Facility to perform logical operations and make decisions based upon predescribed criteria using numerical and nonnumerical data.

A Comparison of Analog and Digital Computer Characteristics
Table 1

8.	Allows the user to experiment by adjusting coefficient settings on the computer, thereby gaining direct insight into system operation.	8. Facility for automatically altering and controlling the topology of the data flow within the machine on the basis of calculations.
9.	Allows the problem to be run in real-time, decreased time[10] (to compress the length of time in which events occur, such as the length of a spacecraft mission), or increased time to expand the length of time in which events occur, such as slowing down the high speed of a chemical process in order to more easily see how the process goes to completion.	9. Eliminates scale factor problems by utilizing floating point number capabilities. Ability to reduce errors inherent in the computer solution by increasing the length of time to obtain a solution.
10.	Stores small amounts of numerical data for short periods of time.	10. Stores any amount of numerical or non-numerical data indefinitely.

A Comparison of Analog and Digital Computer Characteristics
Table 1

Combining the best of the analog and digital machines, the following hybrid computer characteristics are achieved:

1. Combines the speed of the analog computer with the accuracy of the digital computer.
2. Permits the use of analog system hardware in a digital simulation.
3. Increases the flexibility of an analog simulation using digital memory and control.
4. Increases the speed of a digital computation by utilizing analog subroutines.
5. Permits the processing of incoming data which are partially discrete and partially continuous.

Hybrid Computer General Characteristics[1]
Table 2

Other advantages of the hybrid configuration are in the economics of operation (savings of 20/1 to 600/1 have been realized in cases where the hybrid computer had been used in lieu of a general purpose digital computer[4]), and in the efficiency of set-up, checkout, and operation of the analog computer using the digital computer and patchable logic provided in the hybrid system. The features of actual closeness to a physical problem being simulated, the graphical display available only in the analog computer, the man/machine interaction and the ability to plot in real time are retained in hybrid computer simulation.[2,4,8] With hybrid computers the total system simulation capability greatly exceeds that of any single type of machine.[3]

The very nature of the hybrid's digital computer operation - by coded instructions and data - forces each operation to be <u>well</u> documented; this, unfortunately, rarely happens in analog problems.[8] The hybrid computer reduces the chance for human error by providing readout of the analog components as well as control of the analog computer from the digital computer.[12]

C. Hybrid Computer Applications

Numerous applications of the hybrid computer are offered in the literature surveyed. The following is a table of applications from the aerospace, chemical, bio-medical, and communication fields.

Aerospace	1. Aerospace Vehicle Mission Simulations 2. Vertical and Short Take Off and Landing Vehicles. 3. Aircraft Adaptive Control 4. Control System Studies 5. Boundary Value Problems 6. Nose Cone Ablation 7. Launch Window Studies 8. Terrain Avoidance Simulation
Chemical	1. Chemical Reactor Simulations 2. Heat Exchanger Simulations 3. Distillation Columns 4. Kinetics Curve Fitting 5. Process Optimizations 6. Plant Optimization 7. Process Control Simulation
Bio-Medical	1. Electrocardiogram and Electroencephalogram Data Analysis 2. Physiological Simulation
Communications	1. Wave Propagation 2. Ionosphere Ray Tracing 3. Antenna Pattern Calculations 4. Radio Signal Data Processing 5. Learning and Recognition Studies
Others	1. Submarine Simulations 2. Nuclear Reactor Simulations 3. Gas Pipeline Analysis

Hybrid Computer Applications 2, 3, 4, 16
Table 3

One of the major types of problems solved on the hybrid computer is that of physical systems described by partial differential equations. The partial differential equations are reduced to ordinary differential equations for solution on the analog computer as the digital computer holds one variable constant, then stores the solution, updates the variable and recycles for another analog solutions.

Other problems solved by the analog and digital computers operating in closed-loop form are numerical solutions of differential equations, arbitrary function generation, function storage and playback, transport delay simulation, digital computer plant control systems simulation, complex algebraic computations, Boolean Algebra, and Statistical data reduction.[2]

The digital computer is used for solving differential equations whenever the analog computer accuracy is insufficient, or when the problem exceeds the capacity of the analog computer. In aerospace simulations mentioned previously, the spacecraft trajectory equations are solved on the digital computer since they require high accuracy, whereas the spacecraft attitude equations requiring less accuracy are solved on the analog computer.

Statistical problems solved on the hybrid computer include auto and cross-correlation, power spectral density, probability distributions, mean, standard deviation,

feature extraction,[2,4] and Monte Carlo techniques.[1,5,10]

Hybrid computers are becoming increasingly more popular in the universities for simulation of computer-controlled systems; for process control; for instruction in information processing; for computer design; for control system analysis; for the study of digital, analog and hybrid computing systems; and in general, to enable the student to obtain a deeper understanding of the dynamic behavior of physical systems and phenomena.[6]

Other applications are solution of non-linear differential equations requiring maximization or minimization[8], systems of ordinary differential equations with widely different frequencies, faster solution of ordinary differential equations for prediction of system control, analysis and synthesis of pulse-type automatic control systems, filtration and processing of analog and digital data[10], and random search scanning problems[17].

Greater accuracy of a differential equation solution may be attained by using the analog computer to produce corrections to a digitally precomputed approximate solution. This perturbation method may reduce errors below the level of the analog computer accuracy. The analog computer effects only a small correction to the precomputed solution, since the precomputed solution is both drift-free and noise-free[14].

For outstanding in-depth explanations of hybrid computer

applications and methods, the reader is referred to references 1 and 2.

D. Hybrid Computing Systems and Linkages

1. Hybrid Computers in General

Bekey and Karplus[1] define three types of hybrid computer systems:

a. Analog Computer Oriented Systems - the digital computer is used for mode control, pot setting, and generation of special functions.

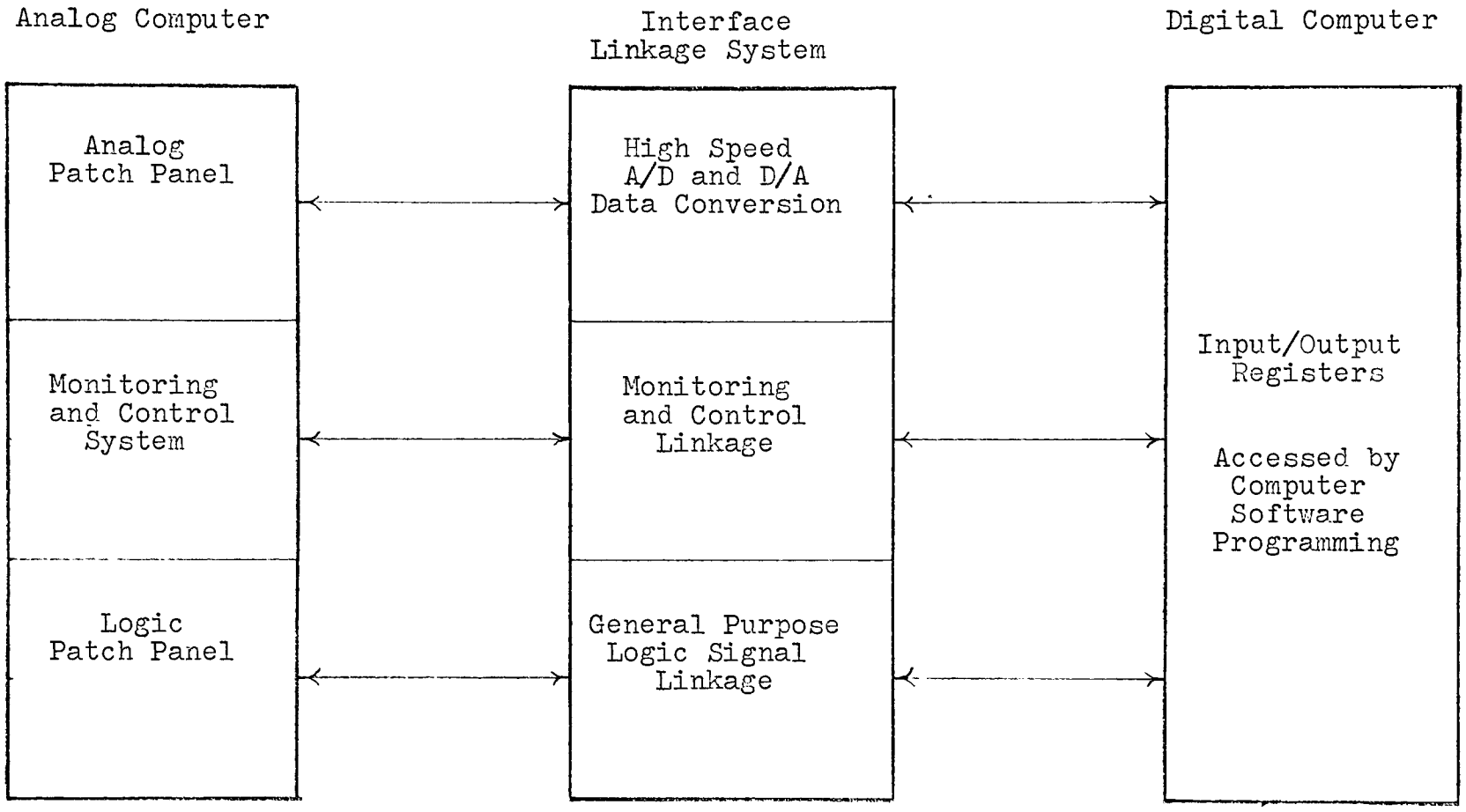
b. Balanced Hybrid Systems - integration and other essential computing functions are performed by both analog and digital computers.

c. Digital Computer Oriented Systems - the analog computer plays a very minor role (perhaps for continuous description of a physical system).

Usually in hybrid systems the digital computer determines the operating characteristics of the overall system in the hybrid mode.

The linkage or interface system is basically what allows the analog and digital computers to "talk" to each other; i.e., it solves the communication problem.[18] The linkage system obviously is very dependent upon the available digital and analog computers and the flexibility in the types of problems to be solved on the hybrid computer. Basic problems that linkage systems must overcome in interfacing a digital computer to an analog computer are problems of voltage and power level conversion, signal buffering, and timing.

Figure 1 is a very simplified block diagram of a typical



Block Diagram of a Typical Hybrid Computer
Figure 1

hybrid computer as partially presented in references 2, 4, and 6.

The purpose of the A/D data conversion is to read into the digital computer the output signals from analog computer components such as amplifiers, multipliers, and resolvers. This is generally accomplished by using a digital code such as binary, binary coded decimal (BCD) or Gray code to represent digitally the analog value of the component. This information can be utilized by the digital computer for processing according to some predesignated digital software program, or stored in the digital computer or its peripheral equipment for later processing.

The D/A channel sends digital information to the analog computer as a result of the A/D information transmitted, or information from the predesignated digital program. This information may be used by the analog computer for changing the state of switches, for component input or output, or for encoding the representative digital value to an analog device.

Frequently the A/D and D/A portion of the linkage system contains timing and multiplex provisions in order that the outputs of more analog components may be sampled rapidly and, greater amounts of data may be transmitted.

The logic signal linkage is used to sense the digital state of a switch or a level comparator on the analog

computer or to control the state of a switch, relay, relay-controlled voltage divider, or analog component such as track/store amplifiers. When used in conjunction with the analog amplifiers and limiters, these lines may be utilized for function generation to take into consideration non-linearities, such as stiction, limiting, gear backlash, hysteresis and dead zone factors. Since the parallel logic is faster than the program controlled digital computer, it is sometimes used for simple functions and control when high speed is desired. The general purpose logic signal linkage may also be used in conjunction with the A/D and D/A conversion and monitoring and control linkage to achieve desired effects. The logic system frequently contains interrupt lines to interrupt the control of the main digital program and force control to another subprogram for calculations or peripheral equipment servicing. The logic signal linkage may also be used for automatic control of the analog computer display devices (Strip chart recorders, X-Y plotters, triggered oscilloscopes, voltmeters), for data reduction, for simulation of discrete logical operations and for hybrid system timing.[6]

In general, the monitoring and control linkage system permits the digital computer to perform automatically the essential functions which the human operator has available on the analog computer control panel.[6] The

Monitoring and Control linkage allows the digital computer to automatically monitor the logical state of switches on the analog computer, as well as the analog voltage output of potentiometers, amplifiers and other analog equipment. This linkage system generally includes a system for addressing the analog component desired and controlling function relays. Addressing is usually accomplished with a stepping switch assembly and driving circuits[5], or with relays, or with electronic switching. The digital computer initiates control of the analog computer modes as a result of the A/D linkage, logic sense lines, monitoring system, or predesignated digital computer program. More generally, the Monitor and Control system permits the analog and digital computers to be controlled by signals originating from either machine. In analog computers with servo setting potentiometers, the communication for the pot setting by the digital computer is handled thru this linkage. The Monitoring and Control linkage often contains the hybrid system clock.

2. Specific Hybrid Systems

A number of commercially manufactured hybrid computer systems and linkages are described in the literature. Appearing in references 1 and 5 are tables of characteristics and pictures of hybrid computers (or analog computers that are used in hybrid systems) manufactured by EAI, Comcor, Milgo Electronic Corporation, Systron-Donner,

Solartron (British), Aritma (Czechoslovakian), VUMS (Czechoslovakian), and Telefunken (German).

The mated hybrid systems are a Beckman Instruments analog computer mated to a Scientific Data Systems (now Xerox Data Systems) digital computer, and an Applied Dynamics analog computer linked to a Digital Equipment Corporation PDP-8 digital computer.

Also, discussed in reference 17 is the Adage 770 hybrid computer linkage system manufactured by Adage, Incorporated. "A distinctive feature of the Adage 770 is the fact that a standard configuration accomplishes all the conversion, control, addressing and timing functions needed for efficient hybrid operation, regardless of the design of the specific digital computer used in the system."

In reference 7, an 18-bit Digital Equipment Corporation PDP/9 digital computer is used in a hybrid system.

The mating of an Electronics Associates Incorporated 680 analog to a Digital Equipment Corporation PDP-8 digital computer (a 12-bit machine) is reported in references 12 and 13. Of interest here is the method of reading from the digital voltmeter the BCD lines available at the DVM connector; this will be discussed under "Systems Concepts".

Discussion of software appears in reference 15 for a hybrid computer system linking an International Business Machines (IBM) 1130 digital computer to an EAI Relay

Mode Control (RMC) TR-48 with a servo-set potentiometer system added. The RIT analog computer is an EAI Electronic Mode Control (EMC) TR-48 without servo set potentiometer capability.

E. Software

Hybrid software is...."the unifying thread which ties together all the subsystems and ensures that the analyst will have programming flexibility which eases his burden while bringing him closer to his model."[16]

Generally, hybrid computers are programmed using a symbolic language such as FORTRAN which makes it convenient for the originator to prepare his own program. The FORTRAN compiler is essential for hybrid programming since most programmers are familiar with that language and most hybrid computer centers are run "open shop" where the originator is able to run his own program. A few hybrid computer centers, however, are run "closed shop". Here the advantage is that the specialized hybrid computer personnel who run the program generally can take full advantage of the system hardware and software capabilities by writing software in assembler language. No matter how efficient a FORTRAN compiler is, software can nearly always be written for more efficient operation by using the digital computer machine or assembly language.

"Since most hybrid applications do not require a large memory for either program instructions or data,

four, eight, or twelve thousand words of core memory should suffice."[3] An exception to this may be the use of sophisticated techniques of numerical integration.

Hybrid software generally falls into three categories - problem preparation, set-up and checkout, and operation.[6]

In the United States Air Force report[11], "A user specifies Software for Hybrid Computing", it is emphasized that inline assembly language programs should be used to meet high speed requirements, but the engineer using the hybrid system is interested in results, and does not want to be bogged down with programming. They suggest using FORTRAN. However, FORTRAN is slower in execution, takes up more core, and does not have all the interrupt service capability as assembler languages.[15]

EAI's HYTRAN software programming system provides a single, unified source language that performs generation of digital codes and analog patching instructions, as well as producing static and dynamic diagnostics for the hybrid program, run time control information for the monitor and for control and timing of the analog and data link equipment.[9]

Other types of hybrid software may be built to calculate time and amplitude scaling, to control peripheral devices, to perform hybrid system and analog programming diagnostics, and to store potentiometer, amplifier and component values on paper or magnetic tapes and files to be used for later hybrid runs.

IV. SYSTEMS CONCEPTS

In the REVIEW OF LITERATURE three types of hybrid computer systems were presented: the analog computer oriented system, the balanced hybrid system, and the digital computer oriented system. The hardware that was available at the beginning of this project and the requirements of the RIT faculty necessitated the building of an analog computer oriented system - that is, one in which the digital computer is used for mode control of the analog computer, potentiometer setting, and generation of special functions. Since the TR-48 does not contain servo set potentiometers, this function must be eliminated from the definition above for our needs. The requirements stated in the section Objectives, to build an interface for mode control of the analog computer and static reading of the potentiometers (pots) and amplifiers (amps), have been combined with the general objectives of flexibility, simplicity, reliability, economy, modularity, and ease of system operation. In order to maintain flexibility, instead of directly connecting functions (other than pot and amp reading & mode control) from the digital computer to the TR-48 or DES-30, general purpose patchable logic lines from the digital computer have been provided. Referring to figure 1, all the general functions of an interface or hybrid linkage system, high-speed A/D and D/A data conversion, general purpose logic signal linkage, and monitoring and control

linkage, have been provided in the RIT hybrid system.

The A/D and D/A data conversion is accomplished using the Hewlett-Packard A/D and D/A converters in the 2116B wired to the TR-48. Eight A/D channels with the provision for software programmable input and multiplexing, and two software programmable positive-voltage D/A channels have been provided. Other than the contribution to the overall hybrid system, these data conversion channels will be of no concern in this thesis.

The general purpose logic signal linkage contains 12 patchable control lines and 12 patchable sense lines between the 2116B and the DES-30.

The monitoring and control linkage consists of a system to address the pot or amp specified by the digital software program and to read the pot or amp value from the analog computer, and a system for controlling the modes of the TR-48 and DES-30.

Highlights of the evolution of this system from the early systems concepts are presented next.

Reading the Potentiometers and Amplifiers

A system had to be devised to read into the digital computer a digital code representing the analog value of voltage present at the output of the potentiometers and amplifiers. A very limited number of inputs to the digital computer were available. The reading could be accomplished by directly connecting a high impedance digital computer A/D input buffer

to every component in the TR-48; this, of course, was out of the question due to the need for many communication lines, input digital registers, and a multitude of wiring internal to the TR-48. A reduction in input buffers could be realized by multiplexing.

On the other hand, the outputs of all the pots and amps were available in digital form at the TR-48 digital voltmeter (DVM)[28]. The problem, if the DVM were to be used, was to find the best way of addressing the pots and amps to reduce the number of communication lines between the 2116B and the TR-48, and to make the analog computer DVM output compatible with the digital computer hardware and software.

References 12 & 13 describe how the problem was solved by The Danish Atomic Energy Commission using a 12-bit DEC PDP-8 digital computer. First, half of the information from the DVM output was strobed into the digital computer and stored, then the lines were switched with logic components for the other half to be read by the same digital computer register. This was quite an elaborate system of gating and timing, and required a number of control lines from the digital computer. This scheme also required a good deal of hardware and quite complicated software, but again this was a 12-bit digital computer.

When the Hewlett-Packard 2116B system was purchased before this thesis began, two digital computer input/output registers were also purchased, one +16 bit duplex register

and one -16 bit duplex register.[22] The 16 bit buffer provides the capability for the 2116B to read 16 bits of information from the buffer or write 16 bits of information to the buffer. It was decided for simplicity to use one of the 16 bit registers to read information from the TR-48 analog computer and DES-30 and one to write out information to the TR-48 and DES-30. Using this technique only 16 bits were available to read the pot and amp values from the TR-48. The DVM reads from -11.999 volts to +11.999 volts; or, since the TR-48 is a 10-volt machine, expressing the DVM readout in machine units (voltage normalized by analog reference voltage), the range of the DVM is-1.1999 to +1.1999 machine units. This information is available at connectors on the rear of the DVM in both a straight decimal code requiring 43 output lines and binary coded decimal (BCD) requiring 20 output lines. Since the code in BCD was a drastic reduction in the number of bits required (lines to the digital computer), it was decided to interface the BCD outputs to the digital computer. The BCD lines required to describe the full range of the DVM are shown in Table 4.

sign bit	1 line
Most significant bit (MSB)	1 line
second MSB	6 lines
third MSD	4 lines
fourth MSB	4 lines
Least significant bit (LSB)	4 lines
Total	20 lines

Number of lines for DVM Output Available in BCD Form Describing the Full Range of the DVM Voltage
Table 4

Since the BCD 8,4,2,1 code contains many redundant bits (for instance, an eight and a four or an eight and a two do not exist simultaneously since this causes a carry to the next highest digit), it was decided to investigate the possibility of using a BCD-to-binary decoder to conserve bits. A survey was made to locate a suitable commercially made BCD-to-binary converter, but none was available. A BCD-to-binary decoder was designed. However, it was shown that a decoder offered only minor savings in bits, while requiring a considerable amount of hardware. A tradeoff study was undertaken to find alternatives to the hardware BCD-to-binary decoder.

Allowing for component drift, the system accuracy of any analog computer is about 1/1000 of the reference voltage. Therefore, the system accuracy of the TR-48 analog computer is approximately .01 volts or .001 machine units. The accuracy of the machine can be described by using up to the fourth most significant bit on the DVM.

The LSB on the DVM readout, it was noted, also shows very little stability from one DVM data conversion to the next. Therefore, the LSB may be dropped without a significant sacrifice in system accuracy.

Dropping the 4 LSB lines decreases the total in table 4 from 20 to 16 bits. This was exactly the number of bits that one 16 bit duplex register is capable of handling. The range of the readout would then become -1.199 to +1.199 machine units.

The range can further be decreased by excluding other information that was deemed not of major concern. The testing of the MSB for a one or a zero indicates whether or not there is a voltage greater than or equal to 10.000 volts, but the voltage on the pots will never become greater than 10.000 volts, 1 machine unit, unless the analog computer reference voltage is set too high.

An amplifier output voltage higher than 1 machine unit would cause an amplifier overload indicator to light; in the static case when the amp is to be read this shows improper analog computer programming. The presence of an overload, and not its magnitude, is of interest. Two of the 2nd MSB lines may be eliminated by excluding the range outside -1.0000 to +1.0000 machine units. This would reduce by two the total number of bits.

Some of the many combinations that were tried were, the dropping of ranges outside $\pm$1 machine unit, the dropping of

the LSB lines and some lines in the 4th MSB digit, and the gating with OR logic information that could not occur simultaneously.

The method that was finally chosen for the RIT digital computer, which is a 16-bit machine, was to limit the range of the DVM output information to -.999 to +.999 machine units with an overflow indicator for greater than or equal to one machine unit. This required one sign bit, one overflow (MSB) bit, four bits to describe the 2nd MSB, four bits to describe the 3rd MSB, and four bits to describe the 4th MSB for a total of 14 bits. The BCD output lines of the DVM are not decoded with hardware, but are sent through buffering to the digital computer where the information is read into the -16 bit register and decoded from BCD to decimal digits by the software.

Schemes for including the LSB in the reading using the current TR-48 and 2116B hardware, but adding more software and interface hardware, are described in the section Recommendations.

Pot and Amp Addressing

The need arose to select the particular potentiometer or amplifier to be read out by the reading system.

Again a minimal amount of bits were available to address a system from the 2116B. Since four bits were needed for mode control, as discussed later in this section, twelve bits were available for pot and amp addressing.

In order to save hardware costs and design time, it was

decided to try to parallel the manual addressing system already provided in the TR-48 and to use as much of the manual system as possible to address the pots and amps automatically from the 2116B.

A description of the manual system may be found in reference 25, p 2.1 to 2.5. In the manual system on the TR-48 control panel, two pushbuttons are provided to select either "P" - pots or "A" - amplifiers. There are 10 buttons 0-9 to address the tens digit of the pot or amp and 10 more buttons 0-9 to address the units digit of the pot or amp. When a pot or amp number is selected the analog voltage value at the output of that device can be displayed digitally on the DVM. When the P or A button is pushed, a relay voltage (20 volts) appears at the tens digit pushbuttons. When the tens digit button is pushed, that relay voltage goes to a relay network that activates all ten components of that tens digit by addressing the trays in which those pots or amps are located. These ten values then appear at the ten units pushbuttons and when one of the units pushbuttons is pushed, that value is sent to the DVM input. For example, if pot #36 were selected, P is pushed which sends the relay voltage to the pots relay network. When the tens digit 3 is pushed, the relays are activated in the pot #30-34 tray and pot #35-39 tray, the values of pots 30-39 appear on the units pushbutton. When the units 6 pushbutton is selected, the value from the pot #36 wiper arm is directed to the DVM

input and the pot setting is displayed.

The objective of the interface addressing system is to accomplish the same initiated automatically from the digital computer.

One way of addressing the pots and amps automatically would be to run a line to each pot or amp individually from the digital computer to switch the component output to the reading system. For RIT's systems this would mean the absurd total of 120 lines. Another way would be to break the lines down into 3 sets - one set of two for the P or A select function, one set of 10 for tens digits 0-9, and one set of 10 lines for the units digit 0-9. This would require 22 lines from the digital computer. But, since only 12 lines were available from the digital computer for the task of addressing, other means had to be found. Using binary coding, the 120 components can be addressed by seven lines or bits, and 22 lines from the 3 sets can be represented with five bits. If the functions are broken down into 3 binary sets as described above and addressed directly, that would be 1 line for the P or A, 4 lines to select the 10 tens digits, and 4 lines to select the 10 units digits for a total of 9 lines or bits. The addressing then can be accomplished using a binary representation with between 5 and 9 lines; this is less than the twelve bits available for the task of addressing.

The objective now was to design the simplest hardware to encode the binary address. Logic systems could be designed

to encode binary to decimal. An electromechanical stepper switch[5] could be used to address the pots or amps.

In reference 29 a system for encoding binary numbers to select lines is described using a diode matrix. In order to address 120 lines a diode matrix with 854 diodes would be required. A 4-line matrix was breadboarded to prove feasibility.

The manual selector system is capable of selecting pots numbered 00-59, and amplifiers numbered 00-79. The current TR-48 installed at RIT includes 45 pots numbered 00-44 and 57 amplifiers numbered 00-74 - some numbers are used to address reference voltages and trunk lines from a remote computer.

In order to use as much of the manual addressing system as possible, it was elected to direct the relay voltage to the TR-48's relay network, much the same way as the manual addressing system does. The functions, however, were broken down into two sets - the pot and amp tens digits, and the units digit.

The amps tens digit required addressing from 0 to 7 or eight lines. It was decided to maintain the capability for addressing as many pots as there are available openings in the TR-48's attenuator panel; this requires selecting pots tens digits for 0 to 5 or six lines. This comes to a total of fourteen lines for the pot and amp tens digit, which is the routing system for the relay network voltage. It was

also decided that the pot and amps tens digit should be addressed automatically by a fourteen-line matrix which requires 56 diodes. This is located on Card #2 and is described later in subsystems details.

The units digit is independent of the type of component selected; it carries the "live" voltage coming from the pot or the amp. For this reason, the voltage switched by the units digit can be switched only with actual switch contracts as opposed to electronic switching devices which would drop the voltage and cause an erroneous reading. The units digit must select ten lines. This requires 4 binary bits which may be decoded using 40 diodes to select the up to 10 lines. This matrix is described later on card #1.

In summary, the addressing system that was selected is comprised of two sets of diode matrices requiring 4 binary inputs, each for a total of 8 addressing bits required from the 2116B to the addressing system.

The addressing system is described in detail under the section SUBSYSTEMS DETAILS and is shown in a block diagram along with the manual addressing and reading system in Figure 12 in the Section REVISIONS TO MANUALS.

Patchable Control and Sense Lines

As stated earlier, the decision to use the one 16-bit duplex register to write and the other to read proved to be very limiting. As it stood, 14 bits of the read register

were taken up by reading the DVM, leaving 2 open bits on the read register, and 4 bits for mode control plus 8 bits for addressing left 4 open bits on the write register.

For hybrid system flexibility a number of free patchable logic lines for function generation and signal reading were desired. Four write bits and two read bits did not seem adequate for this patchable logic capability. At that time a number of systems schemes evolved. The summarization of the evolution seemed to be three states of machine operation - one in which the analog computer was essentially detached from the digital computer, one static state in which the values of the pots and amps could be read out automatically, and one state in which the analog and digital computers were attached for hybrid operation. The registers and lines for this early system would have served a dual purpose; the bits used for addressing and reading required in the static state would be physically switched to other lines to be used during the hybrid operational mode for patchable logic sources and terminations. Schemes for using a manual switch or a relay-actuated multi-bus T-bar switch driven by a command from the digital computer were conceived to switch these bits.

Because the EAI standard tray contains 24 patchable outlets, it was decided to purchase a tray and provide half of these outlets for reading (sensing) and half for writing (control). Expansion to greater capability is discussed

under the section Recommendations.

The patchable logic tray was placed in the DES-30 instead of the TR-48 because the patchable logic bits are digital, because space was available, and because shorter interface cables to the digital computer would be required. Access to the TR-48 can be gained from this patchable logic tray through the DES-30 D/A and A/D trunks on the DES-30 patch panel.

Therefore, in this early system, of the 16 write bits, four would be used for mode control, four more would be used for the patchable logic tray, and eight would be shared between the addressing system and the patchable logic tray, depending upon the state of operation. Of the 16 read bits, two would be used for the patchable mode tray, four would be used for the pot and amp reading system, and ten would be shared between the patchable logic tray and the pot and amp reading system, depending upon the state of operation.

Upon further investigation of the duplex register capability it was decided to use the bidirectional transfer feature of the registers to both read and write. This decision permitted the elimination of the concept of three states of operation. The need to share the bits by a multi-bus switch was eliminated.

The system concept proceeded by assigning the -16 bit register, or DVM register - referenced in the software as 'DVM', to the pot and amp addressing and reading system since the reading system DVM logical voltage level (logical

zero =+2 volts, logical one =-12 volts) was compatible with the -16 bit register logical voltage level. The +16 bit register, or hybrid register - referenced in the software as 'HYBRG', was assigned to the patchable logic tray read and write, and the four mode control (write) bits.

The summary of the system concept for bit allocation is presented in table 5 and table 6.

+16-Bit Register (Hybrid Register)		-16-Bit Register (DVM Register)	
Output (write) bits -			
Patchable Logic	12 bits	Addressing System	8 bits
Mode Control	4 bits		
Total Bits Used	16 bits		8 bits
Unused Bits	0 bits		8 bits
Input (Read) bits -			
Patchable Logic	12 bits	Pot & Amp Reading System	14 bits
Total Bits Used	12 bits		14 bits
Unused Bits	4 bits		2 bits
Total bits used	50		
Total bits unused	14		

Digital Computer ±16 Bit Duplex Register Bit Allocations
Table 5

I. **Channel 14, -16 Bit Register LO = OV, LI = -12V**

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Software Name for this register 'DVM'

A. Output from 2116B

Bit Number	Function	
0	Addressing Units Digit	1
1	Addressing Units Digit	2
2	Addressing Units Digit	4
3	Addressing Units Digit	8
4	Addressing Tens Digit	10
5	Addressing Tens Digit	20
6	Addressing Tens Digit	40
7	Addressing Amps or Pots	

B. Input from DVM BCD output thru buffering Card #3

0	Sign
1	OVERFLOW (10.000)volts
2	1000's 1 = 1 volt = .1 MU (Machine Unit)
3	1000's 2 = 2 volts= .2
4	1000's 4 = 4 volts= .4
5	1000's 8 = 8 volts= .8
6	100's 1 = .1 volt = .01
7	100's 2 = .2 volts= .02
8	100's 4 = .4 volts= .04
9	100's 8 = .8 volts= .08
10	10's 1 =.01 volts=.001
11	10's 2 =.02 volts=.002
12	10's 4 =.04 volts=.004
13	10's 8 =.08 volts=.008

2116B ±16 Bit Duplex Register
Bit Assignments
Table 6
Sheet 1

II. Channel 15, +16 Bit Register, LO=+12v, LI=0V

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Software name for this Register 'HYBRG'

A. Output from 2116B to Mode Control & HYBRID I/O Tray

Bit Number	Function
0	Hybrid Control Bit # 0
1	Hybrid Control Bit # 1
2	Hybrid Control Bit # 2
3	Hybrid Control Bit # 3
4	Hybrid Control Bit # 4
5	Hybrid Control Bit # 5
6	Hybrid Control Bit # 6
7	Hybrid Control Bit # 7
8	Hybrid Control Bit # 8
9	Hybrid Control Bit # 9
10	Hybrid Control Bit #10
11	Hybrid Control Bit #11
12	Mode Control DES-30 CLEAR
13	Mode Control DES-30 RUN
14	Mode Control TR-48 RESET
15	Mode Control TR-48 OPERATE

B. Input from HYBRID I/O Tray

Bit Number	Function
0	Hybrid Sense Bit # 0
1	Hybrid Sense Bit # 1
2	Hybrid Sense Bit # 2
3	Hybrid Sense Bit # 3
4	Hybrid Sense Bit # 4
5	Hybrid Sense Bit # 5
6	Hybrid Sense Bit # 6
7	Hybrid Sense Bit # 7
8	Hybrid Sense Bit # 8
9	Hybrid Sense Bit # 9
10	Hybrid Sense Bit #10
11	Hybrid Sense Bit #11

2116 ±16 Bit Duplex Register
Bit Assignments
Table 6
Sheet 2

Mode Control

The modes of the TR-48 that are to be controlled by the digital computer are Hold, Reset (Initial Conditions), Operate, and Pot Set (required in the reading of the pot values). It is also advantageous to have the Time Scale Fast mode on the TR-48 controlled by the digital computer, especially if the Repetitive Operation (rep-op) mode is programmed. The modes of the DES-30 that are required to be controlled by the digital computer are Stop, Clear, and Run. Again, to conserve hardware, it was desirable to utilize as much as possible the TR-48 and DES-30 existing equipment for mode control. These modes are controlled on the DES-30 by logic levels at the OP, RST, RUN, AND CLR inputs with the exception of the TIME SCALE FAST mode which is actuated on the DES-30 mode control panel by a switch, and the POT SET mode which previously had no link to the DES-30.

Furthermore it is advantageous to control these modes in parallel either from the digital computer as the result of the software program, or from the DES-30 as the result of a logic element output, or from the TR-48 as the result of a logical output such as a comparator. An elaborate hierarchy of control is presented in the sections under Subsystem DETAILS and in the USER'S MANUAL for mode control as a consequence of the parallel mode control design.

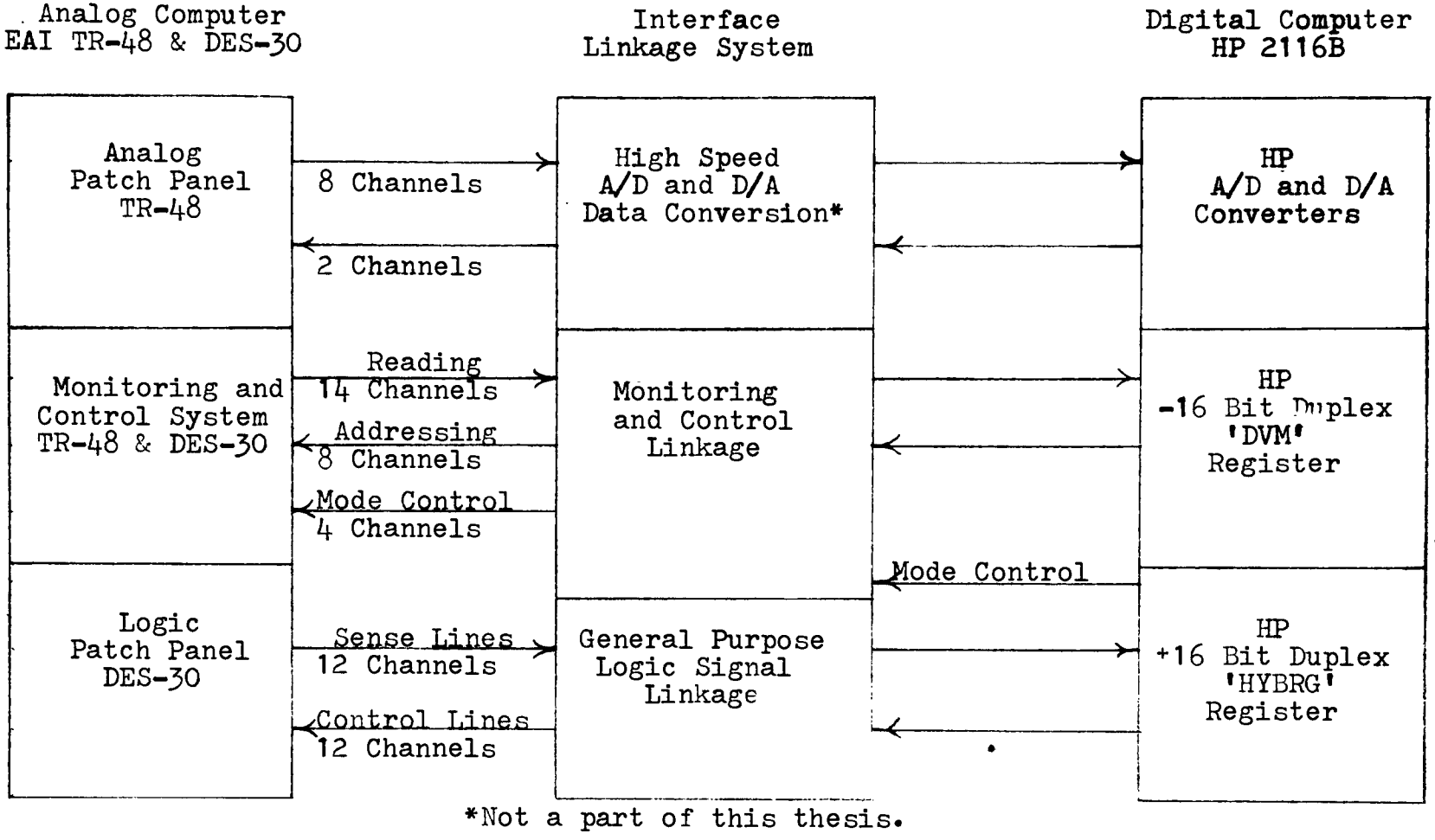
Equipment has been added to control the Pot Set mode and to initiate the Time Scale Fast Mode from a logic level input on the DES-30.

In order to use the digital computer, or the analog computer separately, some convenient means of demating had to be provided. The philosophy in the undertaking of this thesis was to "put the systems back the way they were before they were joined by the hybrid interface." This was accomplished by the use of the ANALOG/HYBRID master switch on the TR-48. This switch has many functions. One advantageous deviation from this philosophy will be discussed later.

Some of the interface lines between the 2116B, TR-48, and DES-30 need not be demated, however, since they play no part in the single system operation. The patchable logic control and sense lines and the reading system from the DVM remain intact when the systems are separated. The pot and amp addressing is de-energized upon separation as well as the digital computer input to the parallel mode control system.

The summary of this system can most easily be depicted by a simple block diagram of the interface system built for this thesis. This appears as figure 2 in the likeness of figure 1.

In conclusion, the system whose evolution is portrayed in this section on system concepts is believed to be one of the simplest, most economical, most flexible, most modular, and easiest to use systems that could have evolved from the available analog and digital computers.



*Not a part of this thesis.

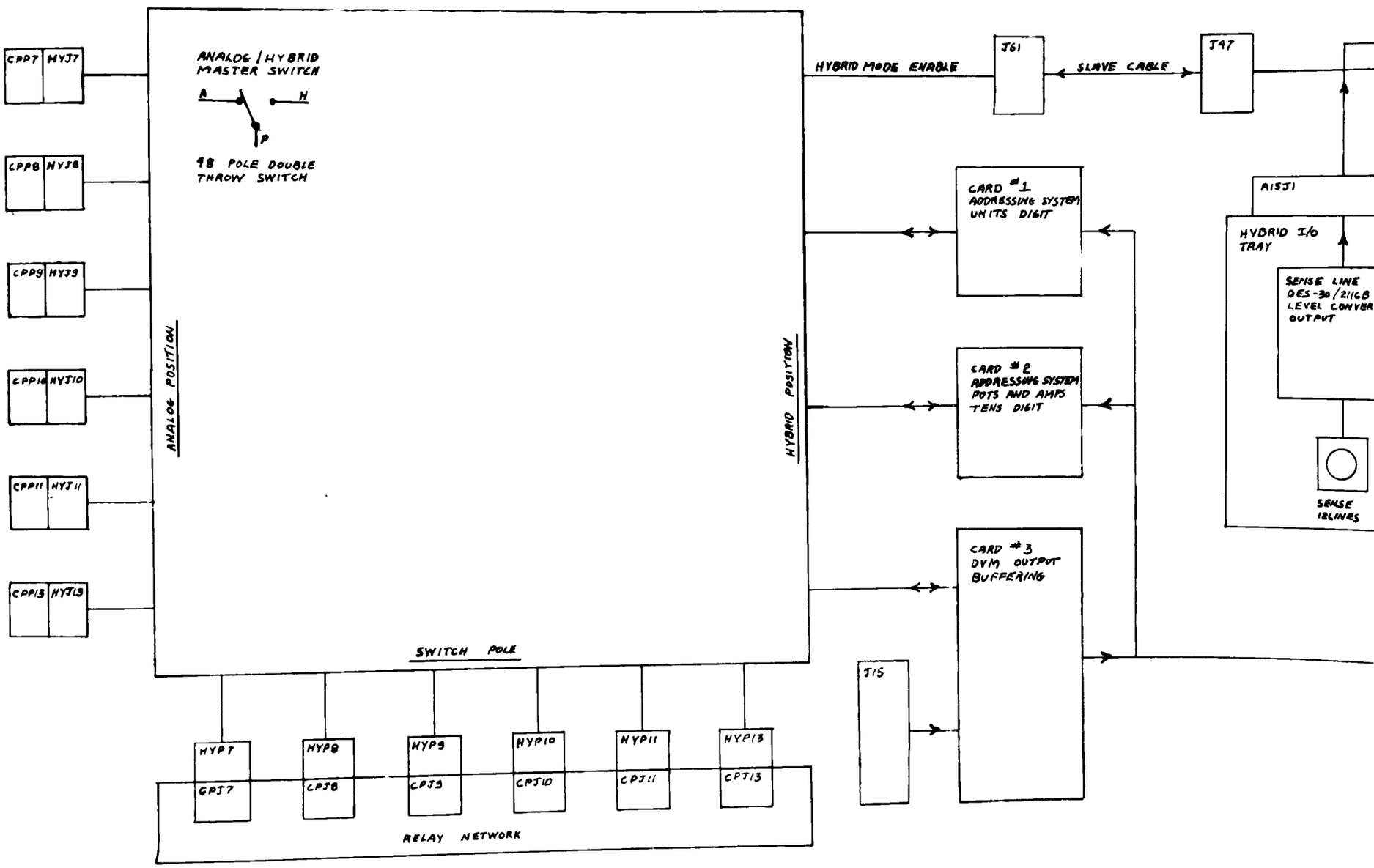
Block Diagram of RIT Hybrid Computing System
Figure 2

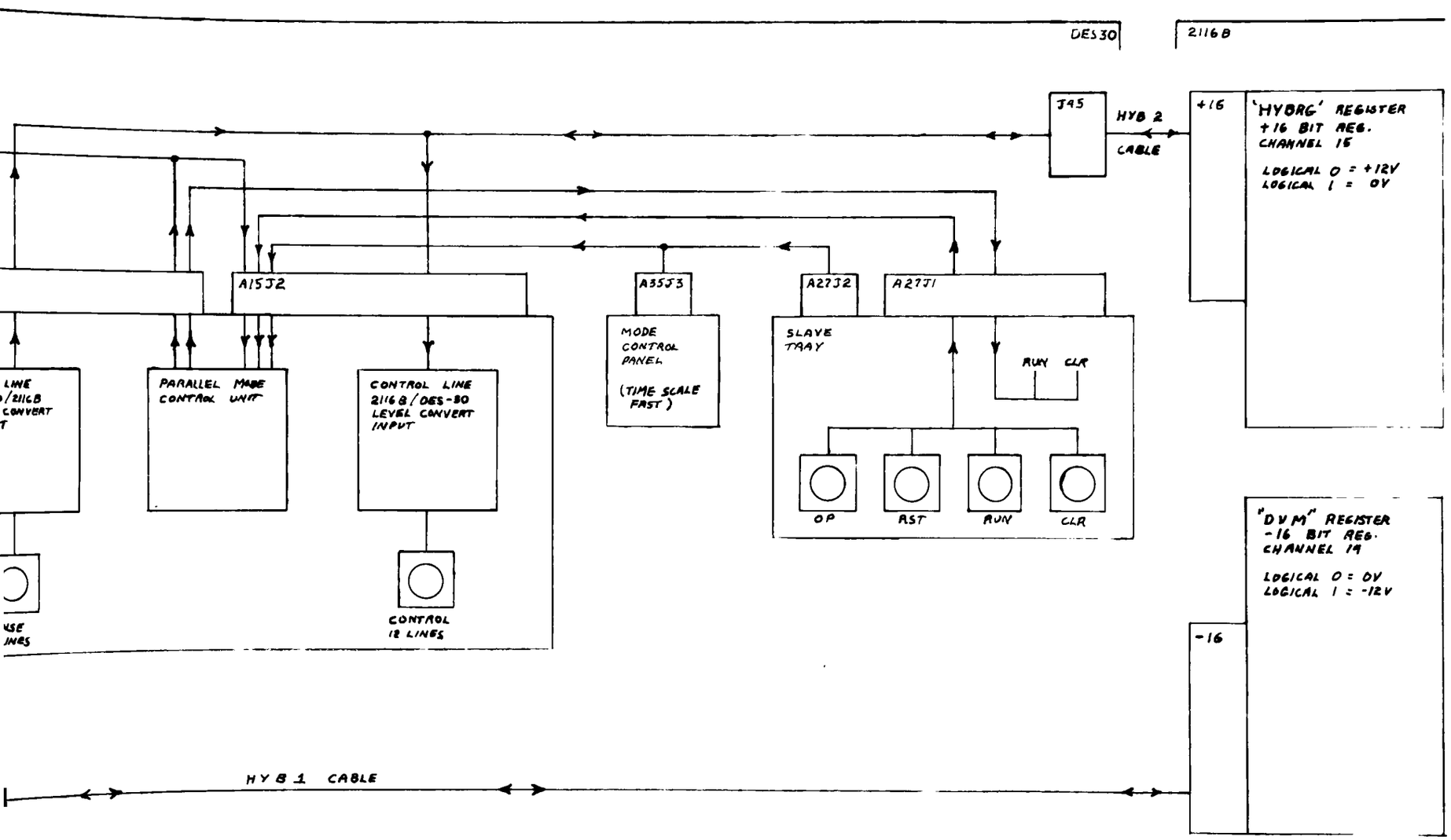
V. SYSTEMS DETAILS

In this section the interconnection is presented. Table 6 is the digital computer ±16 bit duplex register bit assignment list. Figure 3 is the Interface Cable Block Diagram and figure 4 is the Subsystem Interconnection Diagram. The ensuing descriptions can be followed on either of these diagrams; figure 4 is a much more detailed version of figure 3.

The 12 hybrid control lines for the patchable logic originate at the +16 bit duplex register in the 2116B. The logical states on the 12 lines are a result of the software output to the hybrid register. The control lines go from the hybrid register through the HYB 2 cable, through connector J45 on the DES-30 bulkhead, through A15-J2 which is the backplane connector of the Hybrid I/O tray located in Field 1 Bay 5 of the DES-30. In the Hybrid I/O tray at the 2116B/DES-30 Level Convert Input, the logic level of the control lines is changed from the hybrid register logic level, a logical zero = +12 volts and logical one = +0 volts, to the DES-30 logic level, a logical zero = +3.6 volts and a logical one = 0 volts. The electrical current capability of these lines is also matched to the output current of the other DES-30 output elements. The control lines are then terminated on the DES-30 Hybrid I/O tray patch panel block control lines numbered 0 to 11.

The 12 patchable logic sense lines numbered 0 to 11 originate on the DES-30 Hybrid I/O tray at the patch panel block.

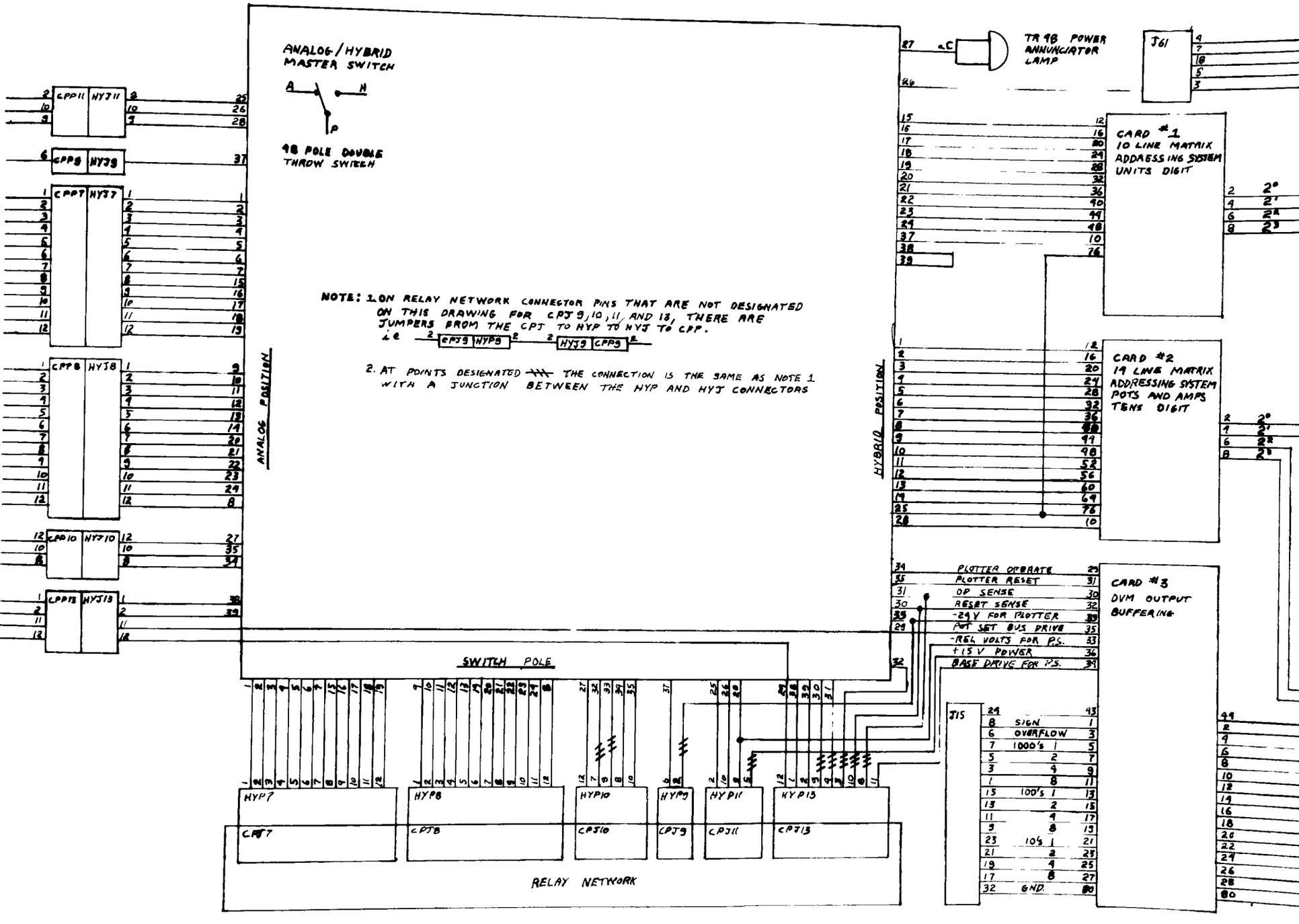

CPPJ7 HYJ7
CPPJ8 HYJ8
CPPJ9 HYJ9
CPPJ10 HYJ10
CPPJ11 HYJ11
CPPJ13 HYJ13
ANALOG / HYBRID MASTER SWITCH
A
H
P
18 POLE DOUBLE THROW SWITCH
ANALOG POSITION
HYBRID POSITION
SWITCH POLE
HYPJ7 CPJ7
HYPJ8 CPJ8
HYPJ9 CPJ9
HYPJ10 CPJ10
HYPJ11 CPJ11
HYPJ13 CPJ13
RELAY NETWORK
HYBRID MODE ENABLE
J61
SLAVE CABLE
J47
CARD #1 ADDRESSING SYSTEM UNITS DIGIT
CARD #2 ADDRESSING SYSTEM POTS AND AMPS TENS DIGIT
CARD #3 DVM OUTPUT BUFFERING
J15
A15J1
HYBRID I/O TRAY
SENSE LINE DES-30/211CB LEVEL CONVER OUTPUT
SENSE LINES

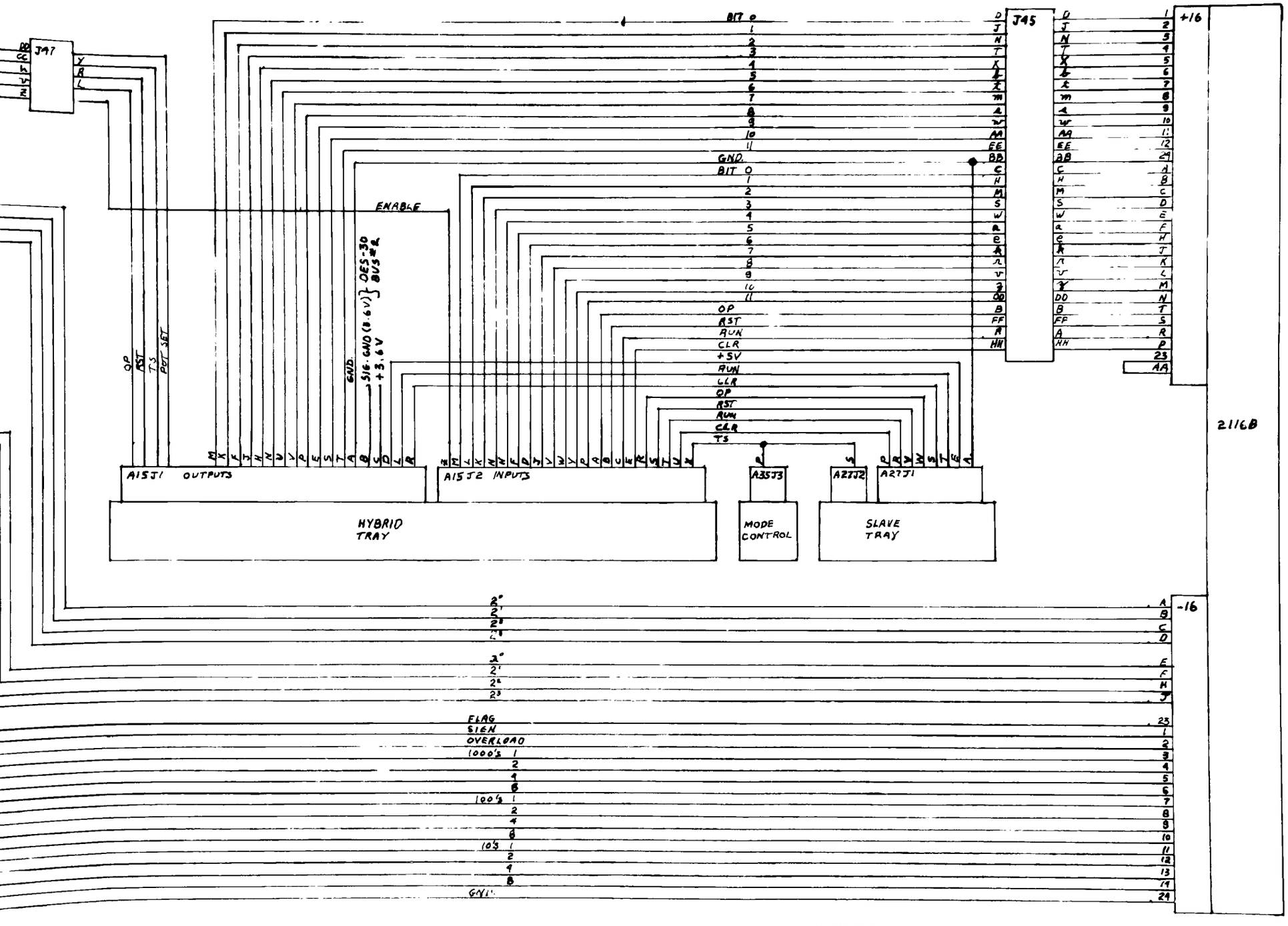


INTERFACE CABLE BLOCK DIAGRAM

FIGURE 3

TR48


ANALOG/HYBRID MASTER SWITCH
A
H
P
98 POLE DOUBLE THROW SWITCH
NOTE: 1. ON RELAY NETWORK CONNECTOR PINS THAT ARE NOT DESIGNATED ON THIS DRAWING FOR CPJ 9, 10, 11, AND 13, THERE ARE JUMPERS FROM THE CPJ TO HYP TO HYJ TO CPP.
CPJ9 HYP9 HYJ9 CPP9
2. AT POINTS DESIGNATED THE CONNECTION IS THE SAME AS NOTE 1 WITH A JUNCTION BETWEEN THE HYP AND HYJ CONNECTORS
ANALOG POSITION
HYBRID POSITION
SWITCH POLE
HYP7
HYP8
HYP10
HYP9
HYP11
HYP13
CPJ7
CPJ8
CPJ10
CPJ9
CPJ11
CPJ13
RELAY NETWORK
TR 98 POWER ANNUNCIATOR LAMP
J61
CARD #1
10 LINE MATRIX
ADDRESSING SYSTEM
UNITS DIGIT
CARD #2
19 LINE MATRIX
ADDRESSING SYSTEM
POTS AND AMPS
TENS DIGIT
CARD #3
DVM OUTPUT
BUFFERING
PLOTTER OPERATE
PLOTTER RESET
OP SENSE
RESET SENSE
-29 V FOR PLOTTER
POT SET BUS DRIVE
-REL VOLTS FOR P.S.
+15 V POWER
BASE DRIVE FOR P.S.
J15
SIGN
OVERFLOW
1000's
100's
GND.



SUBSYSTEM INTERCONNECTION DIAGRAM

FIGURE 1

Inside the Hybrid I/O tray at the DES-30/2116B Level Convert Output, the voltage level is converted from the DES-30 logic level, a logical zero = 3.6 volts and a logical one = 0 volts, to the Hybrid register logic level, a logical zero = +12 volts and a logical one = +0 volts. The input impedance of the sense lines is also made compatible with the 2400 ohm input impedance of all other DES-30 inputs. The converted sense line voltages then go through connector A15-J1 on the back-plane of the Hybrid I/O tray through J45 through the HYB 2 cable to the Hybrid register input where the logic levels of these lines are read into the 2116B and complemented for logical testing by the software program.

The eight pot and amp addressing bits originate in the 2116B software program and are written into the digital computer DVM write register. The lines are carried through the HYB1 cable to the TR-48. Four of these lines go to the 14-line matrix on card #2 for addressing the pot or amp tens digit, and the other four lines go to the 10-line matrix on card #1 for addressing the units digit. The 14-line matrix contains 14 relays, one of which is decoded by the matrix to apply a 20-volt relay voltage through the ANALOG/HYBRID switch to the appropriate bank of relays in the EAI relay network panel. The 10-line matrix contains 10 relays, one of which is decoded to close and carry the voltage of the units digit selected (in combination with the tens digit selected from the 14-line

matrix) back through the relay network panel to the SEL termination on the TR-48 patch panel. If the SEL to DVM bottle plug is in place, the voltage will be applied to the DVM. The DVM converts this analog voltage to a digital value, and displays it on the DVM readout and also applies the BCD representation of that voltage to connector J15 inside the TR-48 cabinet in the rear. The BCD representation of this voltage is contained on 14 lines of connector J15. Since the current drawn by the DVM register is too high for these 14 outputs, the 14 lines are routed to logic card #3 for buffering. The -16 bit register requires an open circuit or -12 volts for a logical one. A transistor switch was placed in each line. These switch buffers which are located on card #3 consume minimal amount of current from the DVM due to the current gain of the transistor. The output of the buffered 14 lines from card #3 goes from the back of the TR-48 through the HYB1 cable to the DVM register in the 2116B. Once the voltage represented digitally on the 14 BCD lines is read into the 2116B, it must be complemented in the software program to account for the initial inversion of the data through the transistors on card #3.

The ANALOG/HYBRID Master switch breaks out these functions from the EAI Relay Network panel required for addressing, mode control, and disabling of the TR-48 manual controls in the Hybrid mode. This switch also initiates an enable line that goes to the parallel mode control and I/O buffer in

the Hybrid I/O tray for enabling the strobing of mode control bits from the 2116B when the switch is in the HYBRID state.

On card #3 are also functions to reset or operate the plotter pen output on the TR-48 patch panel since they are broken out by the hybrid switch as a consequence of the TR-48 manual panel being disabled in the HYBRID mode.

The four parallel mode control bits originate in the HP hybrid register (HYBRG) as a result of the software program output to the register. These lines go through the HYB2 cable, through J45 on the DES-30 bulkhead, through A15-J2 of the Hybrid I/O tray to the parallel mode control and I/O buffer. The four bits from the 2116B designated as OP, RST, RUN, and CLR are joined at the parallel mode control and I/O buffer by the OP, RST, RUN, and CLR bits from the DES-30 Slave tray patch panel (through A27-J1 and A15J2) and the TIME SCALE FAST (TS) bit from the switch on the DES-30 mode control panel through A35-J3 to A27-J2 through A15-J2. In the parallel mode control and I/O buffer these two sets of OP, RST, RUN and CLR bits are combined with the TS bit and the hybrid mode enable bit from the ANALOG/ HYBRID switch to form the logical mode of operation for the TR-48 and DES-30 according to the hierarchy explained in table 9. The results of the parallel mode control logic for the TR-48 are sent to the bus control transistors in the TR-48 through A15-J1 through J47 on the DES-30 bulkhead, through the EAI Slave Cable through J61 on the TR-48 bulkhead through the

the Hybrid I/O tray for enabling the strobing of mode control bits from the 2116B when the switch is in the HYBRID state.

On card #3 are also functions to reset or operate the plotter pen output on the TR-48 patch panel since they are broken out by the hybrid switch as a consequence of the TR-48 manual panel being disabled in the HYBRID mode.

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relay network panel and the ANALOG/HYBRID switch. The POT SET bit also goes to card #3 for conversion to a 20-volt relay voltage. The results of the parallel mode control logic for the DES-30 are sent through A15-J1 through A27-J1 to the place where the original RUN and CLR bits were connected to the DES-30 mode bus drivers.

The joining of the subsystems to the interconnection cables is shown in the next section, Subsystem Details.

VI. SUBSYSTEMS DETAILS

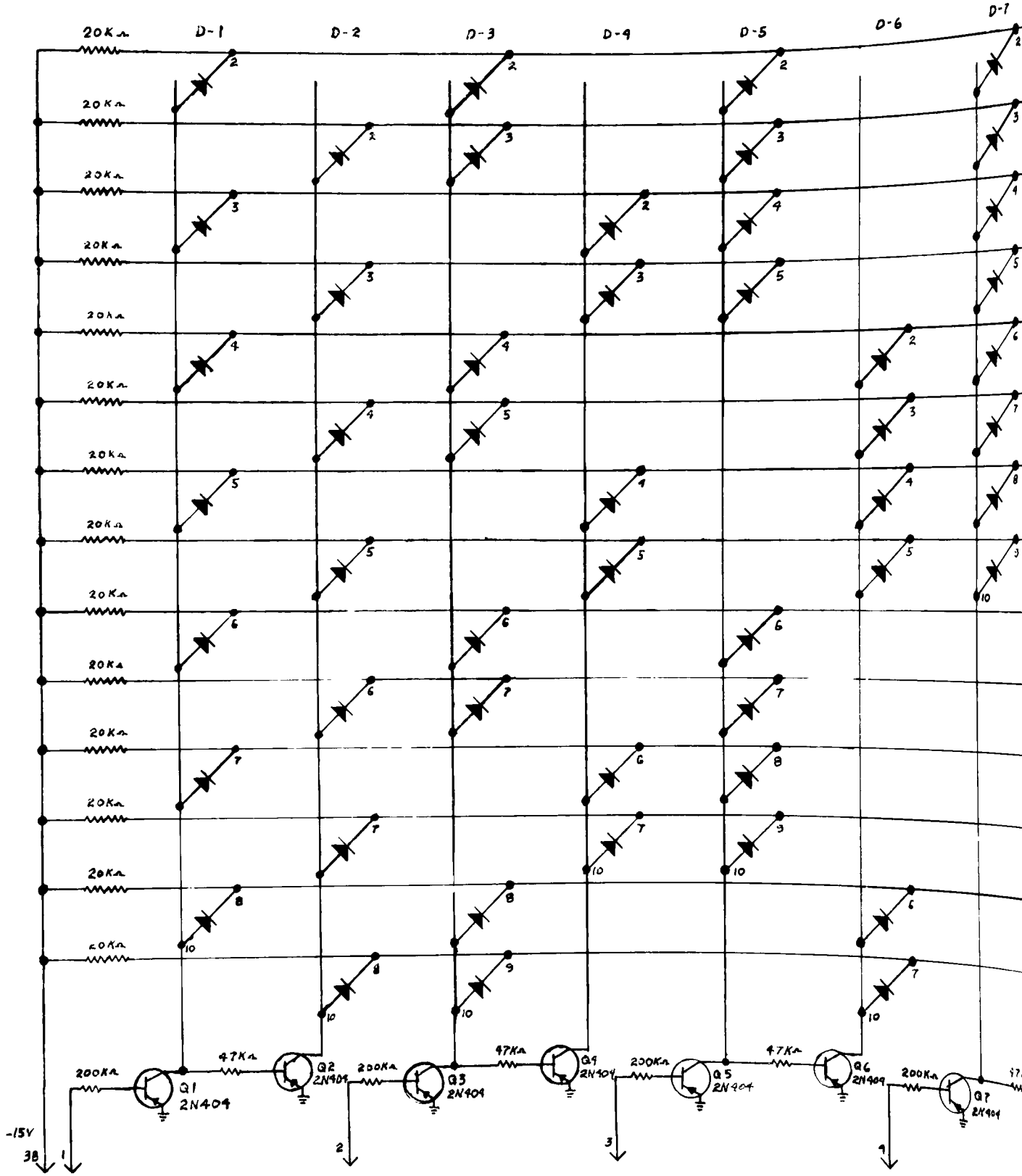
A. Addressing System for Potentiometers and Amplifiers

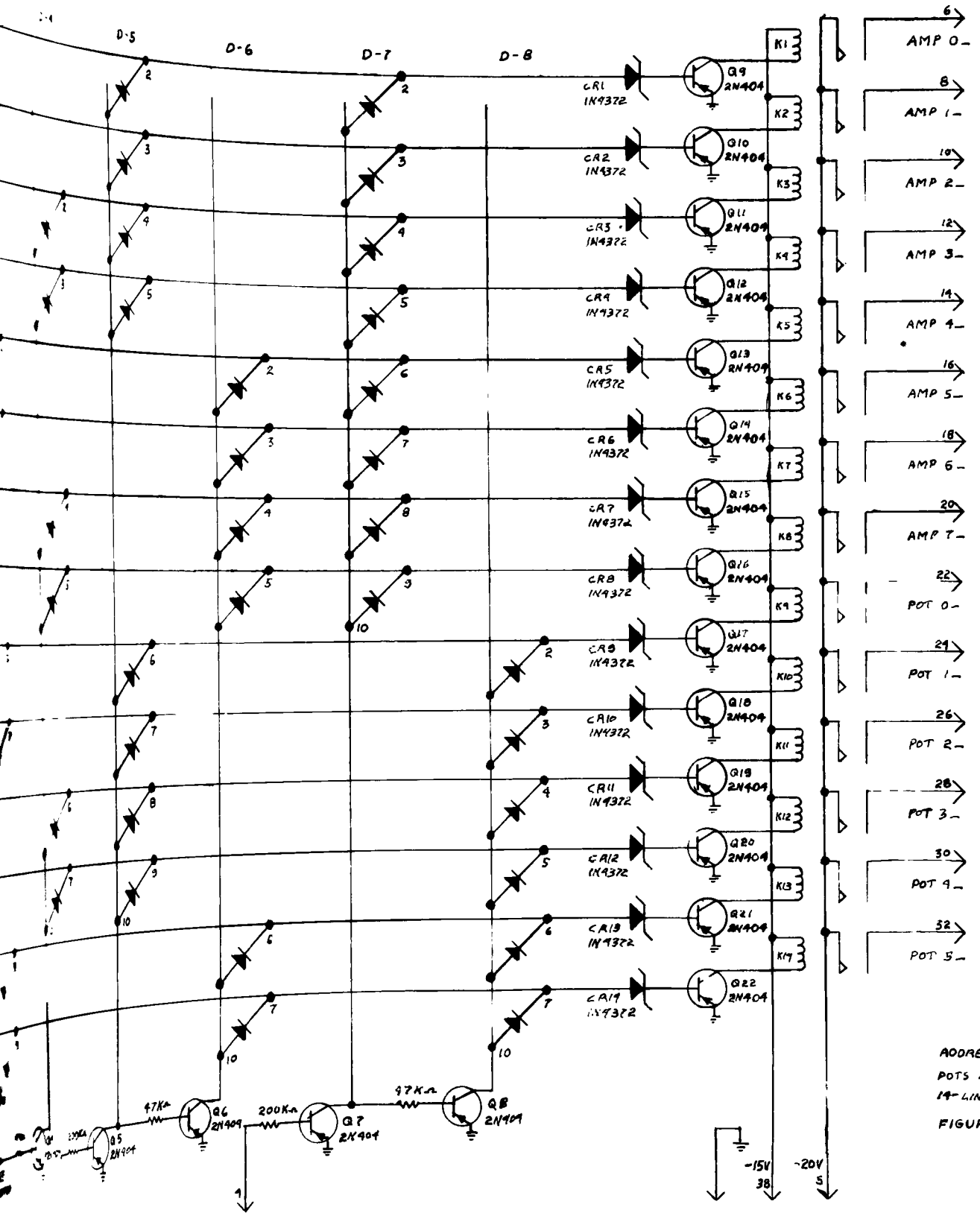
Automatic addressing of the pots and amps from the DVM register is achieved through the use of transistors, relays, diode matrices, and portions of the EAI TR-48 manual addressing system. The nucleus of the Hybrid addressing system is located on card #1 and card #2 inside the TR-48.

Figure 5 is the addressing system diagram for the pots and amps tens digit 14-line matrix located on logic card #2. Figure 6 is the units digit 10-line matrix located on card #1. Figure 12 will also be helpful in understanding the operation of the addressing system.

The addressing system will be explained for selecting pot #36.

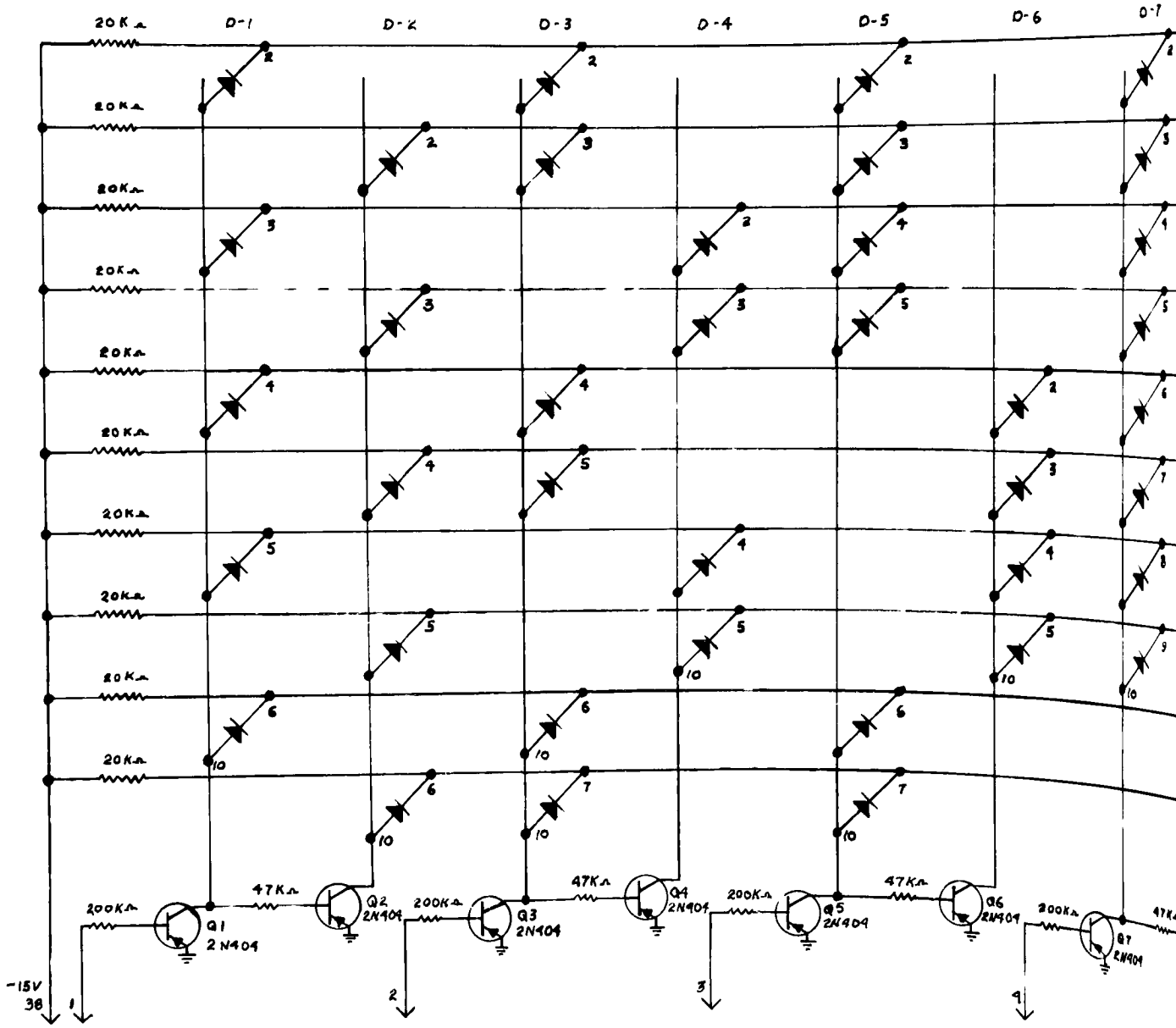
For addressing the pots tens digit, Pot 3_, the binary code for the 2^3, 2^2, 2^1, and 2^0 bits is transferred from bits 7-4 of the DVM register as a result of the software program. Pots are indicated by a one in bit 7 the highest bit. Lines 0-7 on the matrix output are reserved for amplifiers and lines for pots on the matrix output are designated 8-13; therefore, pot 3_ is designated by a 3+8 or 11. The bit structure for pot 3_ is 1011. These bits are applied thru a resistor to the bases of the transistors used for current buffering between

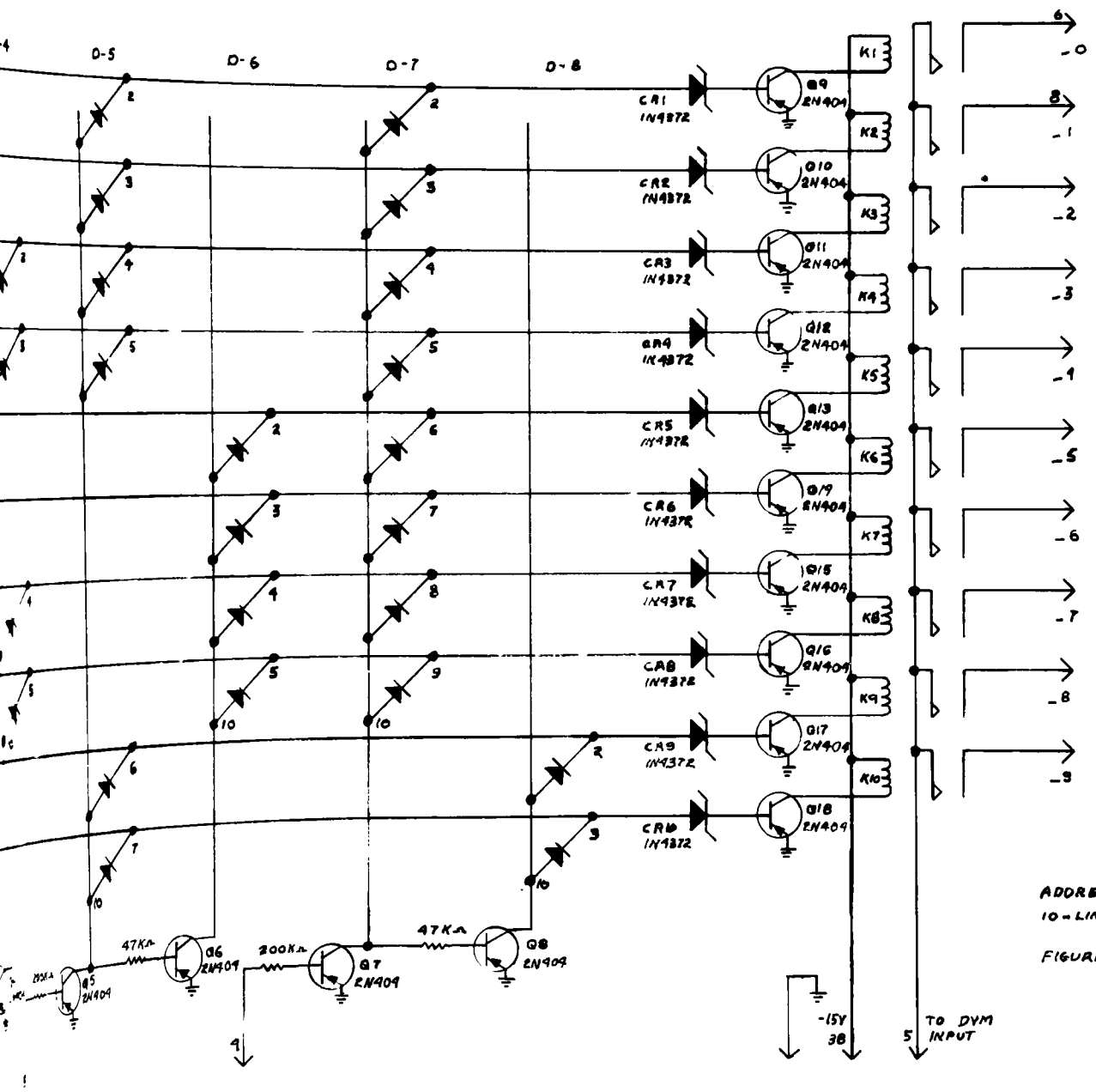

20KΩ
D-1
D-2
D-3
D-4
D-5
D-6
D-7
200KΩ
47KΩ
Q1 2N404
Q2 2N404
Q3 2N404
Q4 2N404
Q5 2N404
Q6 2N404
Q7 2N404
-15V
38
1
2
3
4



ADDRESSING SYSTEM
POTS AND AMPS TENS DIGIT
14-LINE MATRIX CARD #2

FIGURE 5


20K Ω
D-1
D-2
D-3
D-4
D-5
D-6
D-7
200KΩ
47KΩ
Q1 2N404
Q2 2N404
Q3 2N404
Q4 2N404
Q5 2N404
Q6 2N404
Q7 2N404
-15V
38
1
2
3
4



ADDRESSING SYSTEM UNITS DIGIT
10-LINE MATRIX CARD #1

FIGURE 6

the 2116B and diode matrix, and inverting on card #2. The lines are applied at the inverted transistor so the effect through the transistor will be TRUE. Transistor Q_1 will conduct indicating a zero, 0 volts, and causing Q_2 not to conduct indicating a one, -12 to -15 volts. Q_3 and Q_7 also conduct becoming zero and causing Q_4 and Q_8 to become ones. Q_5 will not conduct indicating a one, thereby causing Q_6 to conduct indicating a zero. The true application of the bits to the diode matrix is represented by the states of Q_8, Q_6, Q_4 and Q_2, or 1011. When a one is applied to the input of the diode matrix the diode on that line is clamped to the Zener voltage, 3 volts. However, when a zero is applied to the input of the diode matrix, the diode on that line allows conduction in order to sink the source voltage through its resistor to ground (logical zero). Line 11 has been selected, therefore line 11 goes to the Zener voltage while all other lines conduct, taking that line to ground through the diode.

The transistor at the end of line 11 conducts due to the base voltage and closes the relay in the transistor collector circuit. The relay contacts switch 20 volts to the EAI relay network panel, through the ANALOG/HYBRID switch to the 10-line matrix relay armatures on card #1.

At the 10-line matrix the binary code for _6 or 0110 has been applied to the transistor bases. Going through the transistor inversion and the diodes, line 6 is selected

in the same manner as the 14-line matrix. The transistor at the end of line 6 conducts. The relay switches carrying to the armature common side which is connected to the SEL outlet on the TR-48 patch panel. If the bottle-plug is in place from the SEL to the DVM outlet the voltage is routed to the DVM. The DVM through a perturbation-equalization process[28] digitizes the analog voltage. This digital voltage is displayed on the DVM readout tube and also appears in BCD on connector J15.

The 10-line matrix requires relays in the output since the voltage on the armature is the actual analog voltage from the pot or amp to be read by the DVM. Electronic switching at this point would be much faster than relays, but would drop the voltage that is to be read. The pot and amp reading is required to be done statically; that is, not during the Operate mode, therefore, high speed is not required. Timing in waiting for the relays to flip and settle (approximately .3 milliseconds) is accomplished by the Hybrid System Executive Software. Though the 10-line matrix requires relays, electronic switching could be utilized in the 14-line matrix for switching the 20-volt relay voltage to the situs. However, using electronic switching here would increase the speed of the system very little since the digital computer must also wait for the 10-line matrix relays to switch. It was also advantageous to make the 10-line and 14-line matrices as similar as possible for design, maintenance and component

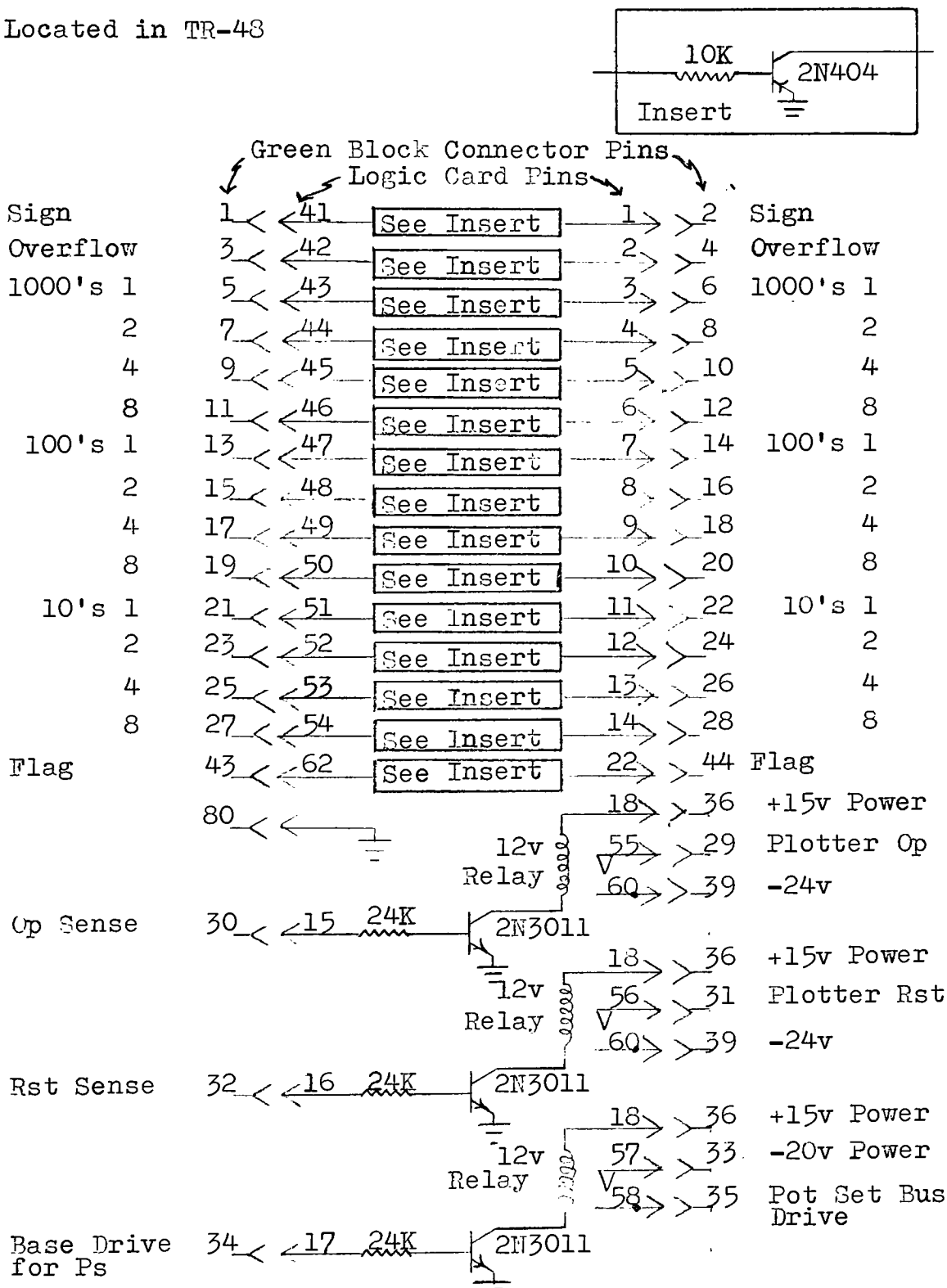
standardization.

The addressing system hardware provides the capability to address Pots 0 to 59, and Amps 0 to 79. The Hybrid System Executive Software provides the capability to address Pots and Amps from 0 to 99.

B. Reading System for Potentiometers and Amplifiers

The pot and amp reading system utilizes the BCD output available at the rear of the DVM. There are 14 bits used to describe the DVM output representing the voltage on a pot or an amp. The reasoning behind the readout character structure was discussed under SYSTEMS CONCEPTS. The reading system buffers are located on card #3 inside the TR-48.

The reading system merely permits the digital computer to read the digital representation of the pot or amp voltage from the DVM. The BCD outputs from the DVM have a logic level of logical zero = +2V, and a logical one = -12 volts. Due to the similarity in logic levels between the DVM output and the -16 bit duplex DVM register (where a logical zero = 0v and a logical one = -12v), it would appear that these lines could be connected together directly, however, the DVM register requires approximately 12 milliamps (ma) current and the DVM output is capable of only about 5 ma. On card #3, figure 7, transistor buffering is provided between the DVM output and the DVM register input. The DVM register in the digital computer operates on



DVM Output Buffering Card #3
Figure 7

internal voltage sources; when the external device is a logical zero (grounded) this internal voltage source is sunk through an internal resistor to the logical zero ground, and another internal voltage source provides the base drive for a transistor. When the external device is a logical one (a threshold voltage above ground), the internal voltage is not grounded and serves to clamp the internal transistor in a reversed bias condition.[22] The logical one voltage of -12 volts is not so sacrosanct, the only thing that matters as far as the register is concerned for a logical one to appear is that there is not a grounded or nearly grounded low voltage (up to 2.5v magnitude) condition on the external device. For this reason, an open circuit works just as well for a logical one as a voltage source. Card #3 provides transistors that for all practical purposes reflect either an open circuit or a grounded (closed) circuit to the DVM register. The DVM output provides the base drive current of approximately .1 ma through a resistor to switch the transistor whose current gain provides the 12 ma required by the duplex register. Of course, there is a logical inversion due to these transistor buffers in the 14 lines. This inversion must be taken into account by the Hybrid System Executive Software program.

C. Parallel Mode Control

The parallel mode control unit is an extension of the

mode control that is available between the DES-30 and slaved TR-48. The parallel mode control unit is located inside the DES-30 Hybrid Tray which was designed for this project. In the EAI system, four logic level inputs on the DES-30 slave tray control the modes of the TR-48 and DES-30. Reference 24 shows the EAI mode control operation (reproduced in table 7) before the interface system parallel mode control modification was added.

TR-48 Mode Control			DES-30 Mode Control		
OP	RST	RESULTING MODE	RUN	CLR	RESULTING MODE
0	0	HOLD	0	0	STOP
0	1	RESET (IC)	0	1	CLEAR
1	0	OPERATE	1	0	RUN
1	1	Not Allowed*	1	1	Not Allowed*

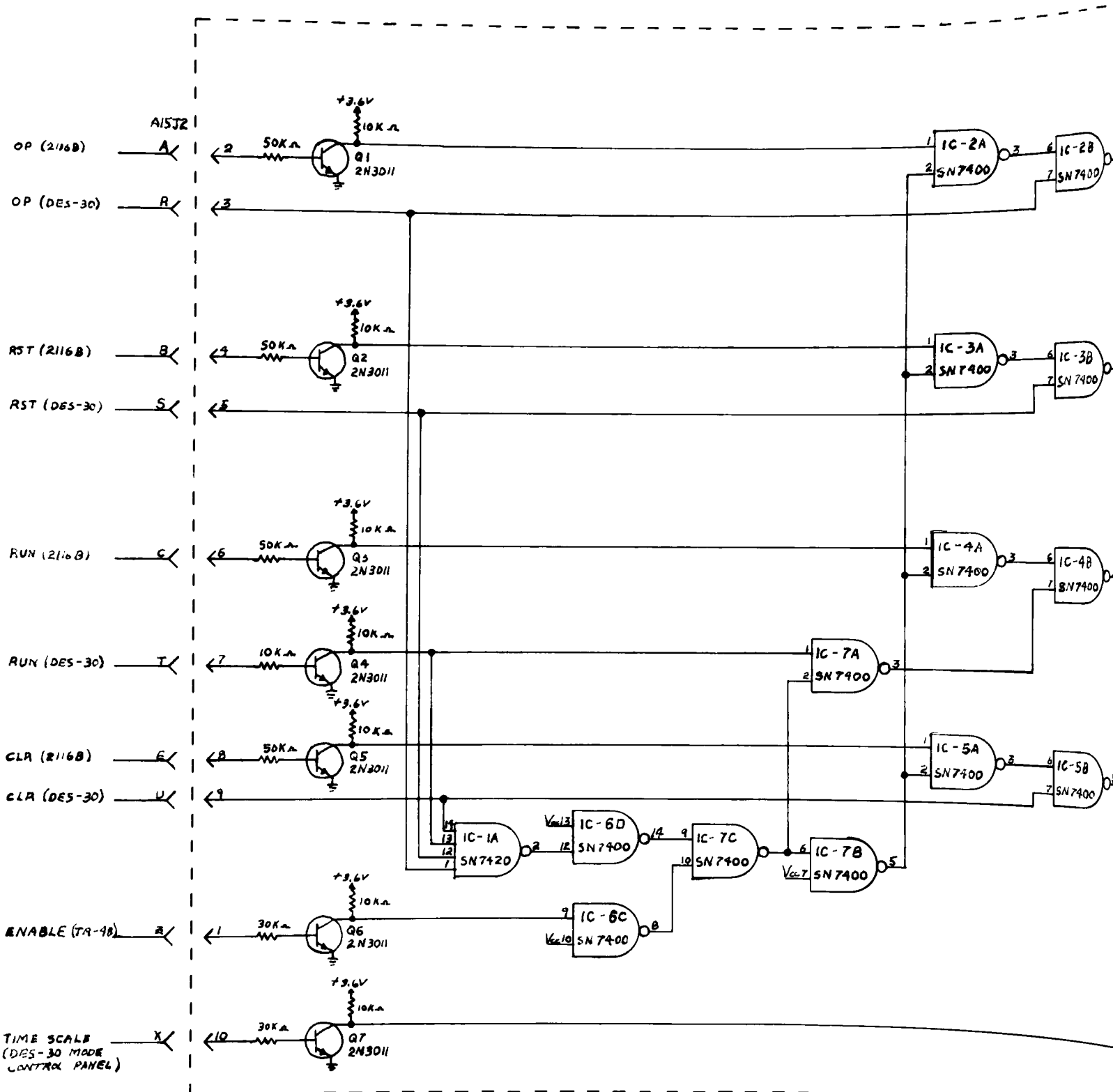
Previous Mode Control Truth Table
Table 7

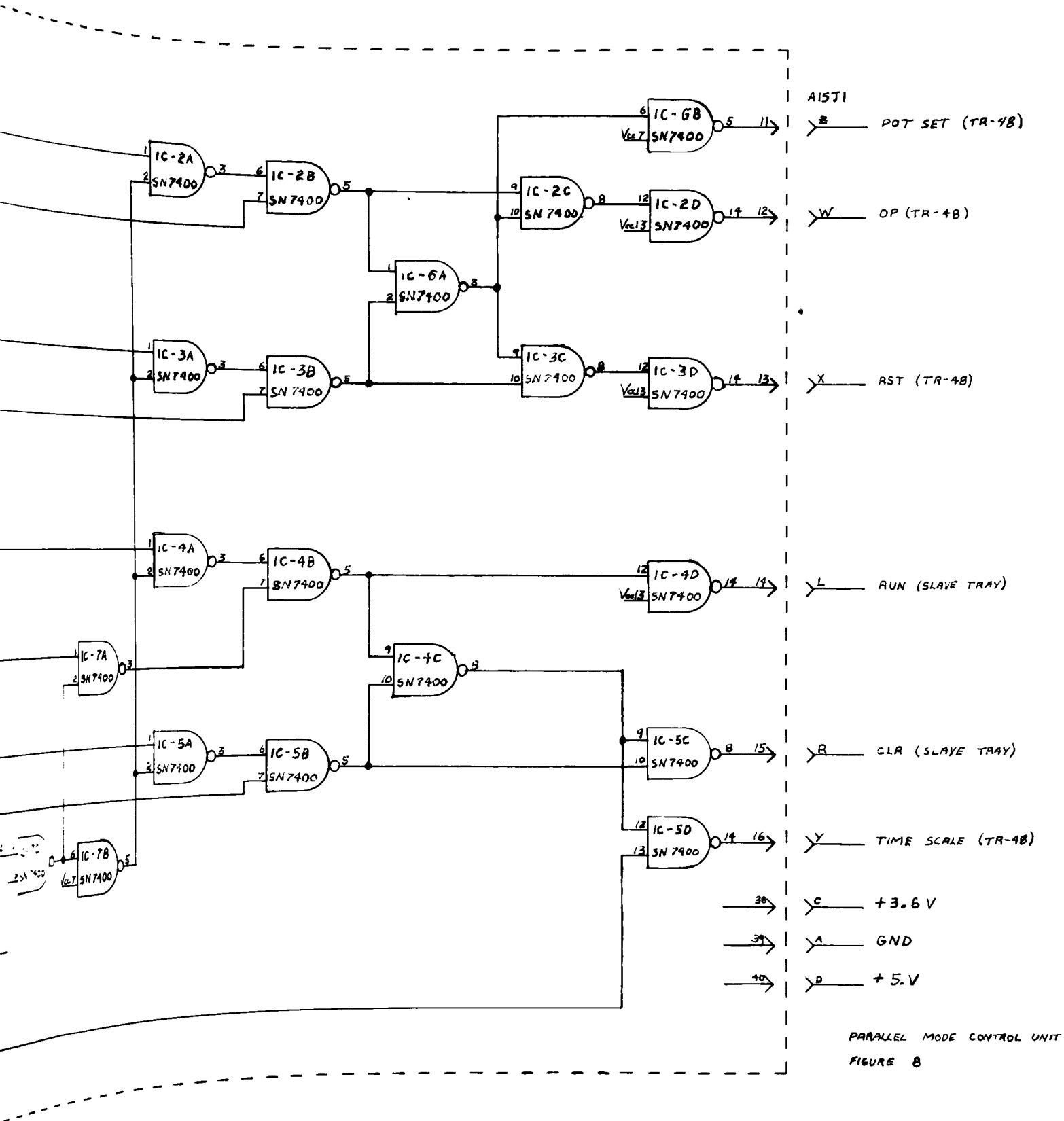
The states marked with an asterisk (*) have been altered by the parallel mode control unit to provide the TR-48 POT SET mode under TR-48 MODE control, and the TR-48 TIME SCALE FAST (TS) under the DES-30 Mode Control. The reader must understand that the TS mode is not a DES-30 mode. The only time the TS mode would logically be selected is when the DES-30 is in the RUN mode; the RUN and TS mode can exist simultaneously in this code. The all possible combinations of modes is presented in Table 9 of the USER'S MANUAL Section VII in this thesis. When the system is operating in the Hybrid mode, the digital computer assumes control of the TR-48 and DES-30 modes

according to the truth table as a result of the user's software program and the Hybrid System Executive Software. There is one exception: in the Hybrid mode, if any of the DES-30 patch panel inputs becomes a logical one on the OP, RST, and CLR inputs or the RUN input becomes a logical zero at the slave tray, control of the TR-48 and DES-30 is shifted from the digital computer to the DES-30 patch panel. In this way the TR-48 and DES-30 may be controlled as the result of a logic element output on the DES-30 or a comparator on the TR-48 patched through the trunk lines and the DES-30 patch panel. The big advantage to this control hierarchy is that the user need not patch a logic element or comparator output to one of the patchable logic sense lines, constantly test that sense line with the software in a loop and then initiate control of the TR-48 or DES-30 from the digital computer software - the control can be made directly from the DES-30 patch panel with a considerable savings in software and in the time necessary to initiate the action. An example of this technique follows. Suppose the system is in the HYBRID mode and the digital computer has controlled the TR-48 into the operate mode and the DES-30 into the run mode. The user specifies the analog solution to proceed until the output of a certain amplifier reaches a specific voltage. The output of the amplifier can be wired to one of the TR-48 comparators where the voltage

is compared to the specified voltage set into the comparator output will become a logical one. The comparator output is sent to the DES-30 via a trunk line. The trunk line termination on the DES-30 patch panel is patched to the RST bit and the CLR bit and the inverted output of the trunk line termination is patched to the RUN bit on the Slave Tray. When the amplifier voltage is reached, the TR-48 will take control from the digital computer and change the TR-48 mode from operate to reset and the DES-30 from Run to Clear.

Figure 8 is the logic diagram of the parallel mode control unit located in the DES-30 Hybrid I/O Tray. Nand logic was used for the parallel mode control since it was in stock. One set of the OP, RST, RUN, CLR bits is obtained from the DES-30 Slave Tray patch panel block, the other set is derived from bits 15-12 of the Hybrid register from the 2116B as a result of the Hybrid System Executive Software. The software sends the bit structure to the parallel mode control unit. A buffer transistor changes the logic level from the Hybrid register logic, logical zero = +12 volts and logical one = +0 volts, to the NAND logic level. The bits from the DES-30 slave tray already correspond to the inverted Nand logic voltage level. The NAND logic is a logical zero = 0 volts, and a logical one = between approximately 3.2 and 5.5 volts.[30] Referring to figure 8, the 4 bits from the digital computer are gated


A15J2
OP (2116B)
A
OP (DES-30)
R
RST (2116B)
B
RST (DES-30)
S
RUN (2116B)
C
RUN (DES-30)
T
CLR (2116B)
E
CLR (DES-30)
U
ENABLE (TR-48)
Z
TIME SCALE (DES-30 MODE CONTROL PANEL)
X
+3.6V
10K Ω
50K Ω
30K Ω
Q1 2N3011
Q2 2N3011
Q3 2N3011
Q4 2N3011
Q5 2N3011
Q6 2N3011
Q7 2N3011
IC-1A SN7420
IC-2A SN7400
IC-2B SN7400
IC-3A SN7400
IC-3B SN7400
IC-4A SN7400
IC-4B SN7400
IC-5A SN7400
IC-5B SN7400
IC-6C SN7400
IC-6D SN7400
IC-7A SN7400
IC-7B SN7400
IC-7C SN7400



PARALLEL MODE CONTROL UNIT

FIGURE 8

by the condition that 1) the computer is in the HYBRID mode, evidenced by the appearance of a logical one, +5 volts, on the enable bus as a result of the ANALOG/HYBRID switch being in the HYBRID position, and 2) the OP, RST, CLR inputs from the DES-30 slave tray patch panel are at a logical zero level, +3.6 volts and the RUN input is at a logical one, 0 volts. Next, the four bits from the digital computer are OR'ed with the four bits from the slave tray. If both the OP and RST bits are a logical one, output to the operate and reset are inhibited and output is sent to the POT SET bus; otherwise, the OP and RST bits pass normally to their respective TR-48 buses. Since there is no 20-volt relay voltage source available in the DES-30, the low-voltage logic signal from the POT SET output is sent back to the TR-48 where the voltage is converted on card #3. If both the RUN and CLR bits are a logical one, output to the RUN bus is enabled, but output to the CLR bus is inhibited and output is made to the Time Scale Fast Bus in the TR-48. Otherwise, the RUN and CLR bits are passed back to their respective buses in the DES-30 Slave tray. The TS bus bit generated from the RUN and CLR bits is also OR'ed with the TS bit from the DES-30 mode control panel switch TIME SCALE FAST/NORMAL.

D. Hybrid Patchable Logic Control Lines

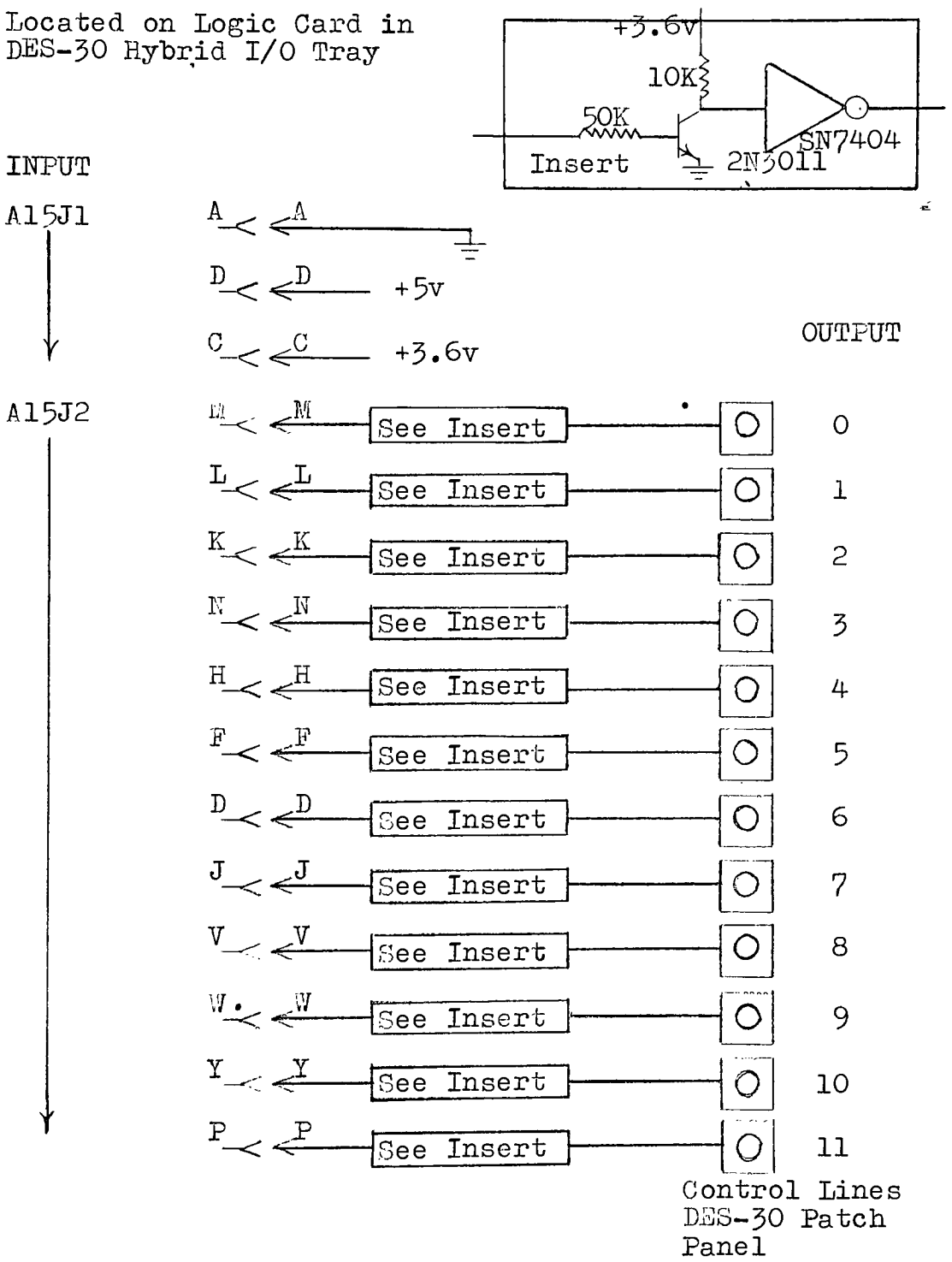
The 12 control lines originate at the Hybrid Register. The logic levels on these lines are the result of output

to the Hybrid Register from the Hybrid System Executive Software. The methods of controlling these by the software is explained in sections under SOFTWARE and in the USER'S MANUAL. The control line buffers and terminations are located in the DES-30 Hybrid Tray.

The output bit structure of the hybrid register comes through these lines to the Hybrid I/O Tray in the DES-30. Inside the tray the logic levels are converted by transistors and inverters in the control line 2116B/DES-30 Level Convert Input unit, figure 9. This converter changes the HP Hybrid register logic level, logical zero = +12 volts and a logical one = +0 volts, to the DES-30 patch panel logic level, where a logical zero = +3.6 volts and a logical one = 0 volts. The output current capability (36 ma) of the Hybrid patchable logic control lines is also increased to at least that of the other DES-30 outputs. The converter also provides inversion of the signal thereby eliminating the need for software initialization of the control lines; the initial state of the control lines is a logical zero. The converted control lines then terminate in the Hybrid I/O patch panel block-control outputs numbered 0 to 11.

E. Hybrid Patchable Logic Sense Lines

The 12 sense lines originate at the DES-30 Hybrid I/O tray patch panel block sense inputs numbered 0 to 11. The logic levels on these lines are the result of inputs



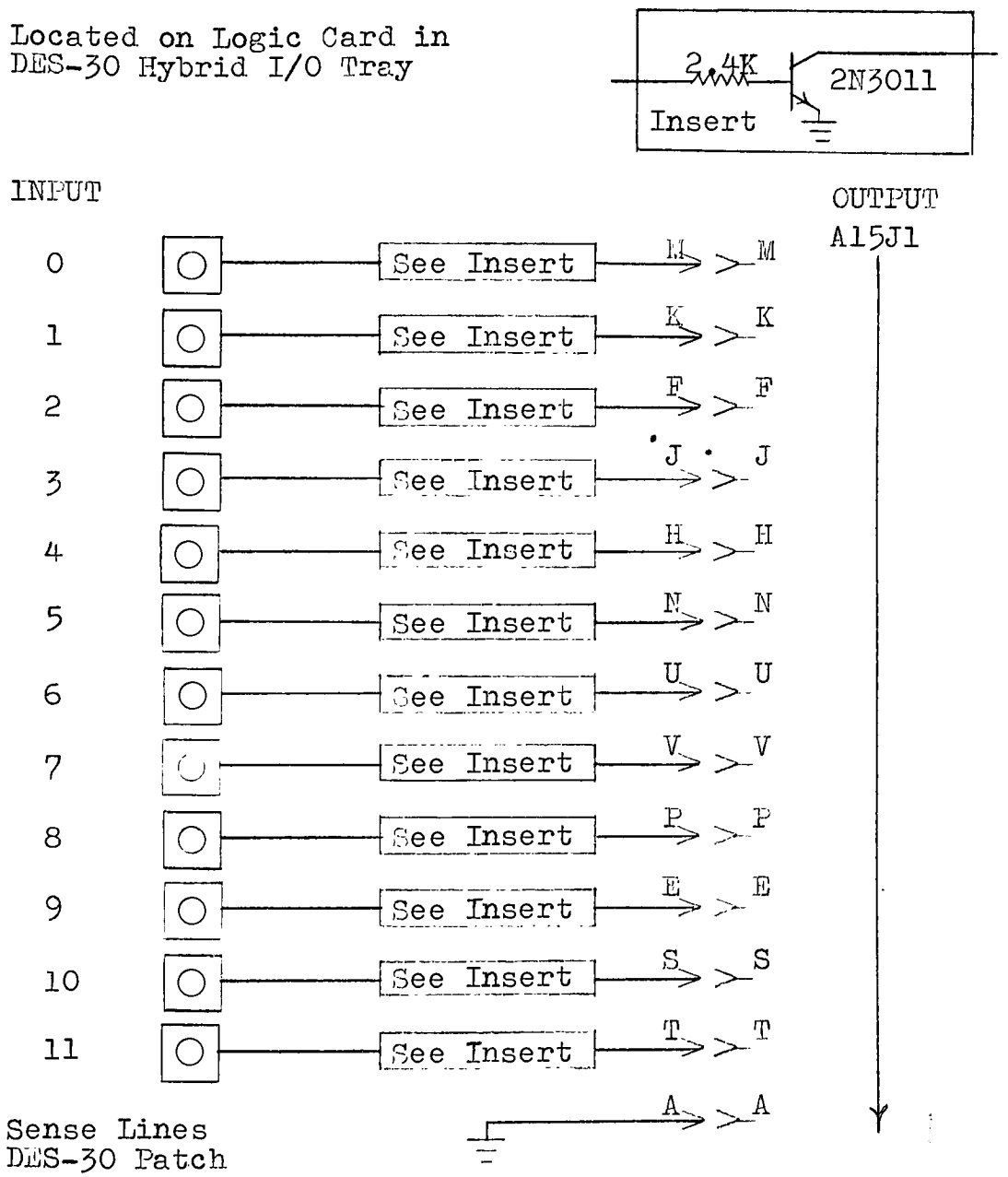
Control Line 2116B/DES-30 Level Convert Input
Figure 9

from the DES-30 patch panel or from the TR-48 through the trunk lines and DES-30 patch panel. Inside the Hybrid I/O tray at the sense line DES-30/2116B Level Convert Output, figure 10, the logical level of the DES-30, a logical zero = +3.6 volts and a logical one = 0 volts, is converted by transistor buffers to the logic level of the HP Hybrid register where a logical zero = +12 volts and a logical one = 0 volts. The input impedance of the Hybrid Sense lines is also made comparable to the input impedance of the other DES-30 patch panel inputs. The converted sense lines then go to the digital computer hybrid register where the information on these lines is automatically software inverted and may be tested by the user's program using the Hybrid System Executive Software as explained in the section under software and in the USER'S MANUAL.

F. ANALOG/HYBRID Master Switch

The ANALOG/HYBRID Master Switch is a 48 pole double-throw, break-before-make switch located on the TR-48 upper panel in the left-hand bay. This switch is used to mate the 2116B, DES-30, and TR-48 for Hybrid operation, and demate them for Analog operation. Table 8 is a functional listing of the switch poles, ANALOG throw side, and HYBRID throw side. The switch wiring may also be found on figure 4.

When the ANALOG/HYBRID switch is switched to HYBRID,



Sense Line DES-30/2116B Level Convert Output
Figure 10

Terminal #	Connection to Pole (Armature)	Connection during HYBRID Mode	Connection during ANALOG Mode	Function
1.	HY P7-1	Card #2 12	HYJ7-1	Amps 10's digit 0_
2.	2	16	2	Amps 10's digit 1_
3.	3	20	3	Amps 10's digit 2_
4.	4	24	4	Amps 10's digit 3_
5.	5	28	5	Amps 10's digit 4_
6.	6	32	6	Amps 10's digit 5_
7.	7	36	7	Amps 10's digit 6_
8.	HY P8-12	40	HYJ8-12	Amps 10's digit 7_
9.	1	44	1	Pots 10's digit 0_
10.	2	48	2	Pots 10's digit 1_
11.	3	52	3	Pots 10's digit 2_
12.	4	56	4	Pots 10's digit 3_
13.	5	60	5	Pots 10's digit 4_
14.	6	64	6	Pots 10's digit 5_
15.	HY P7-8	Card #1 12	HYJ7-8	Unit's digit _0
16.	9	16	9	Unit's digit _1
17.	10	20	10	Unit's digit _2
18.	11	24	11	Unit's digit _3
19.	12	28	12	Unit's digit _4
20.	HY P8-7	32	HYJ8-7	Unit's digit _5
21.	8	36	8	Unit's digit _6
22.	9	40	9	Unit's digit _7
23.	10	44	10	Unit's digit _8
24.	11	48	11	Unit's digit _9
25.	HYP11-2	Card #1 76 &2	HYJ11-2	-15 volt power source
26.	10	J61 3	10	+5v Hybrid Mode Control Enable
27.	HYP10-12 TR-48 Power Annunciation Lamp contact AC	Open	HYJ10-12	Mode indicator lamp power
28.	HYP11-9 Card #3-33	Card #2-10	HYJ11-9	-20 volt power source
29.	HYP13-12	Card #3-35	Open	Closes Pot Set Slaveline by shorting INT switch

30.	9	HYP13 -10	Open	Closes Reset Slaveline by shunting INT switch
		Card #3-32	Open	Reset Mode Sense for Plotter
31.	4	HYP13 -8	Open	Closes Operate Slaveline by Shunting INT Switch
		Card #3-30	Open	Operate Mode Sense for Plotter
32.	HYP10-7	HYP13 -3	Open	Closes Time Scale Slaveline by Shunting INT Switch
33.	HYP10-9		Open	-24 volt source
		HYP9- 2 Card #3 39		Turns on Slave Mode for DES-30 Plotter Mode Drive
34.	HYP10-8	Card #3-29	HYJ10-8	Plotter Operate
35.	10	31	10	Plotter Reset
36.		SPARE		
37.	HYP 9-6	Card #1-10	HYJ 9-6	DVM Selector line input
38.	HYP13-1	Shorted to A/H Switch Term 39	HYJ13-1	DVM input, Mode Control panel bypass
39.	HYP13-2	Shorted to A/H	HYJ13-2	DVM input, Mode Control panel bypass
40.-48.		SPARE		

ANALOG/HYBRID Master Switch
Table 8

essentially all the manual selector functions for the pots and amps, as well as all the mode control functions are shifted to the digital computer executive control. The switch cancels the functions of the TR-48 selector and mode control switches so that they do not interfere with the mating to the digital computer. There is no need to retract or cancel these switches manually. The ANALOG/HYBRID master switch when thrown to HYBRID takes the TR-48 from the INT - internal position - and places it into the slave mode HD/SL to the DES-30. So that the user does not have to cancel all these switches, and so that the user does not interfere when the digital computer has control in the Hybrid mode, the ANALOG/HYBRID switch totally disables the selection and mode control switches on the TR-48 control panel. In order for the user to gain control back from the digital computer, he need only enable the TR-48 control panel by flipping the ANALOG/HYBRID switch back to ANALOG. The user can also gain mode control in the HYBRID mode from the digital computer by patching the switches at the top of the DES-30 or the logical one output on the DES-30 Slave Tray into the appropriate OP, RST, CLR termination on the Slave Tray.

If it is desired to read a pot or an amp while the system is in the HYBRID mode the bottleplug may be removed from the SEL to DVM on the TR-48 patch panel and the output of the appropriate pot or amp patched directly to the

DVM input. The pots should never be patched to the VM termination, due to the voltmeter input impedance; however, the amplifier output may be read using the voltmeter. Of course, if the true coefficient of the potentiometer is to be read in this manner from the pot arm when the TR-48 is not in the Pot Set mode, the voltage on the pot must be removed and the reference voltage, 10 volts, applied.

The concept of separating those functions of the analog computer and digital computer indicative of the hybrid mode when not in the hybrid mode is deliberately violated by the parallel mode control unit. The added capability of the selection of the pot set mode and the time scale fast mode from the OP, RST, RUN, and CLR bits on DES-30 remains when the TR-48 and DES-30 are used separate from the 2116B. However, since the user following an EAI manual which has not been updated for this system and who knows nothing of these capabilities will never tap into these modes, it is felt that this violation is justified.

VII. USER'S MANUAL

In this section are presented the FORTRAN callable subroutines available for Mode Control, Potentiometer and Amplifier Reading, and Hybrid Mode I/O Patchable Sense and Control lines. Instructions for operating the system and suggestions for using the system are also presented.

This section has been written to be used independent from this thesis as a User's Manual for quick reference in programming and operating the Hybrid system.

SUMMARY OF HYBRID SYSTEM LIBRARY SUBROUTINES - CALLABLE FROM HP FORTRAN

I. MODE CONTROL

A. CALL HOLD -TR-48
B. CALL RESET -TR-48
C. CALL OP -TR-48
D. CALL POTST -TR-48
E. CALL STOP -DES-30
F. CALL CLEAR -DES-30
G. CALL RUN -DES-30
H. CALL TS -TR-48
I. CALL MODE (IBITS)

$0 \leq$ IBITS $\leq 15_{10}$ Base Ten Integer Equivalent of Binary

J. CALL TIMER

II. Potentiometer and Amplifier Reading

A. CALL POT (NUMP)

$0 \leq$ NUMP $\leq 44_{10}$ Base Ten Integer

B. CALL AMP (NUMA)

$0 \leq$ NUMA $\leq 74_{10}$ Base Ten Integer

III. Hybrid Mode I/O Patchable Tray

A. CALL CONT (NUMOT, ISTAT)

$0 \leq$ NUMOT $\leq 11_{10}$ Base Ten Integer Number of Line Controlled

ISTAT { 0, 1 } Specified Value of State to Which the Line Is To Be Controlled

B. CALL SENSE (NUMIN, JSTAT)

$0 \leq$ NUMIN $\leq 11_{10}$ Base Ten Integer Number of Line Sensed

JSTAT { 0, 1 } Returned Value of State of Line Sensed

C. CALL ALCON (JOUT)

$0 \leq$ JOUT $\leq 4095_{10}$ Base Ten Integer Equivalent of Binary

D. CALL ALSEN

Hybrid System Library Subroutines Called From FORTRAN Programs

I. MODE CONTROL

Mode Control of TR-48 and DES-30 commanded from the 2116B.

The following programs control the states of the DES-30 and TR-48 provided: (1) the Analog/Hybrid Mode switch is in the Hybrid Mode and (2) the inputs OP, RST, RUN, and CLR on the DES-30 Slave Tray are not patched (or in a logical 0010 state respectively if they are patched) and (3) the DES-30 Mode Control Panel is in the RUN state. The TR-48 is set to HOLD and the DES-30 is set to STOP automatically as the initial state of the Hybrid System.

A. CALL HOLD

Places the TR-48 in the Hold mode; e.g., stops the analog program solution, and maintains the voltages attained to that point in the solution.

B. CALL RESET

Applies the initial condition voltages to the integrating amplifiers on the TR-48. If this mode is called during the solution of an analog problem, the problem is reset to the starting point and held there.

C. CALL OP

Solution of the analog problem on the TR-48 commences when this mode is selected; e.g., the integrators are simultaneously released to respond to input voltages.

D. CALL POTST

The potentiometers on the TR-48 have a +10 volt reference applied to the high side so that the coefficient setting may be read out from the arm of the potentiometer. All the input resistor summing junctions of the amplifiers are grounded so that the potentiometer setting can be read under the loaded condition.

Exception: The last pot in every bank of five pots is ungrounded, and there is no reference voltage applied to the pot during the POTST Mode. If the setting of these pots is desired, a 10 volt reference must be patched to the high side of the pot and the low side of the pot must be patched to ground while the pot setting is read out from the pot arm. These pots are numbered 4, 9, 14, 19, 24, 29, 34, 39, 44.

E. CALL STOP

The DES-30 is placed into the STOP Mode. All clocked elements on the DES-30 maintain their most recent state (similar to the Hold on the analog computer).

F. CALL CLEAR

All DES-30 clocks are inhibited; flip-flops, registers, and counters are cleared.

G. CALL RUN

The DES-30 clock is applied to all clocked (Red colored output) logic elements.

H. CALL TS

Time Scale Fast

Reduces the size of the TR-48 integrator feedback capacitors by a factor of 500, thereby increasing the speed of the analog solution. This mode is also available on the DES-30 Mode Control panel, Analog Time Scale Bus Control "FAST". The size of the integrator capacitors may also be reduced by a factor of 10 independently of the TS mode by removing the plug covering the .1B cross-hatched area on the 12.1322 Electronic Dual Integrator Network in the TR-48 patch bay. The DES-30 will be set to the RUN mode, if it is not already in the RUN mode, when the TS (Time Scale Fast) mode is selected. To turn the TS bus from fast to normal use CALL RUN.

I. CALL MODE (IBITS)

Any of the above modes may be called serially, however, if it is desired to call two or three modes simultaneously the subroutine MODE may be used. The argument IBITS is an integer base ten number set in the calling program and transferred to the Hybrid Library subroutine according to the modes selected from the following truth table:

$0 \leq IBITS \leq 15$

IBITS (base ten integer)	Equivalent Binary OP RST RUN CLR	MODES TR-48/Time Scale/DES-30		
0	0000	HOLD	NORMAL	STOP
1	0001	HOLD	NORMAL	CLEAR
2	0010	HOLD	NORMAL	RUN
3	0011	HOLD	FAST	RUN
4	0100	RESET	NORMAL	STOP
5	0101	RESET	NORMAL	CLEAR
6	0110	RESET	NORMAL	RUN
7	0111	RESET	FAST	RUN
8	1000	OP	NORMAL	STOP
9	1001	OP	NORMAL	CLEAR
10	1010	OP	NORMAL	RUN
11	1011	OP	FAST	RUN
12	1100	POTST	NORMAL	STOP
13	1101	POTST	NORMAL	CLEAR
14	1110	POTST	NORMAL	RUN
15	1111	POTST	FAST	RUN

Mode Control Hierarchy
Table 9

J. CALL TIMER

This program provides a waiting period of approximately 100 milliseconds until the next FORTRAN statement is executed on the digital computer.

II. POTENTIOMETER AND AMPLIFIER READING

In the Hybrid Mode, the value of any pot or amp may be read out by the 2116B statically using the following FORTRAN callable subroutines from the Hybrid System Library. Note: a jumper must be placed between the SEL and DVM terminations on the TR-48 patch panel before these programs are executed.

A. CALL POT (NUMP)

Argument NUMP is the potentiometer to be read out. NUMP is a base ten integer $0 \leq NUMP \leq 44$ since there are only addresses to 44 on the current TR-48.

Subroutine POT first checks to see that the TR-48 is in the Pot Set Mode, and calls POTST if it is not. POT then addresses the potentiometer specified to be read out in NUMP through the Hybrid Addressing System. POT then reads the value of the pot from the TR-48 Digital Voltmeter, and prints out the pot number and its value on the Teletype. If more than one pot is to be read, the user again calls POT from his FORTRAN program, a series of pots can be read by indexing NUMP in a DO LOOP.

B. CALL AMP (NUMA)

Argument NUMA is the amplifier to be read out. NUMA is a decimal integer. $0 \leq NUMA \leq 74$ since there are only addresses to 74 on the current TR-48.

Subroutine AMP first checks to see that the TR-48 is in the Reset Mode, and calls RESET if it is not. AMP then addresses the amplifier specified to be read out in NUMA through the Hybrid Addressing System. AMP then reads the value of the amplifier from the TR-48 Digital Voltmeter, and prints out the amplifier number and its value on the Teletype. If more than one amplifier is to be read, the user again calls AMP from his FORTRAN program, a series of amplifiers

can be read by indexing NUMA in a DO LOOP.

The positive and negative reference amplifier output voltages can be read by addressing AMP (48) and AMP (49).

The fifteen IN-TRUNKS on the TR-48 patch panel may be read out by addressing AMP (50) to AMP (64).

III. HYBRID MODE PATCHABLE TRAY

A Hybrid tray is located in the DES-30. This tray has 12 inputs which can be individually addressed by the 2116B. These inputs and outputs may be patched to the DES-30 registers, flip-flops, counters, or logic elements. The addressed bits may also be patched to the Slave or Trunk Tray D/A Trunks for controlling TR-48 switches, track/store functions and individual integrators. The read bits may be patched to read a signal from one of the DES-30 patch panel outputs or the TR-48 electronic comparators through the A/D trunks.

A. CALL CONT (NUMOT, ISTAT)

This subroutine addresses the Hybrid bit specified by NUMOT and places it to the state specified by ISTAT.

NUMOT and ISTAT are both Integer base ten numbers.

$$0 \leq \text{NUMOT} \leq 11$$

CONT outputs the bit from the 2116B to the DES-30. ISTAT, the bit logical state, then appears at the designated bit NUMOT in the green

colored section of the HYBRID I/O Tray. The contol lines are all set to a logical zero as the initial state of the Hybrid System.

B. CALL SENSE (NUMIN, JSTAT)

This subroutine addresses the Hybrid Tray bit number specified by NUMIN, reads the logical state of this bit in the orange colored area of the Hybrid I/O Tray, and transfers that state thru the argument JSTAT back to the user's FORTRAN program for calculations and decisions. If the SENSE line is not patched the logical state of JSTAT will be returned as 1.

$0 \leq$ NUMIN ≤ 12 Bit number specified

C. CALL ALCON (JOUT)

The state of any one of the Hybrid bits may be addressed and changed serially by the subroutine CONT. However, if it is desired to change two or more of the bits at the same time, the subroutine ALCON is used. Where JOUT is the bit structure of all twelve binary bits stated in base ten integer.

$$0 \leq \text{JOUT} \leq 2^{12}-1 = 4095$$

for example

JOUT = 4095 sets all twelve bits to a logical one state simultaneously, 111111111111

D. CALL ALSEN

The state of any one of the 12 Hybrid bits may be tested using the subroutine SENSE. However, if it is desired to read all 12 bits at once, the subroutine ALSEN is used. ALSEN reads the Hybrid bit structure from the Hybrid Tray in the DES-30, and prints out the bit structure on the Teletype unit.

INSTRUCTIONS FOR OPERATING THE SYSTEM

It is assumed that the user has prior knowledge of the TR-48[23], DES-30[24], 2116B[21], and the FORTRAN programming Language[21].

First, a Hybrid program is written in FORTRAN using the necessary FORTRAN statements and the Hybrid System Executive software FORTRAN callable subroutines listed on the Summary Page and explained in detail on the preceeding pages. The program is punched onto optical sense cards using a keypunch or the cards may be marked manually. The program is compiled on the digital computer which provides a punched paper tape binary output. The tape is loaded into the digital computer using the HP Basic Control System Software. Then the TR-48 and DES-30 are activated. The three systems are then mated by switching the ANALOG/HYBRID Master switch to the HYBRID position for control of the TR-48 and DES-30 by the digital computer as determined by the FORTRAN program.

A sample program for reading 10 pots and 10 amps follows:

Column

1 7

```
FTN,L,B
      DO 1 NUM = 1,10
      CALL POT (NUM)
      CALL AMP (NUM)
1     CONTINUE
      STOP
      END
      END$
      blank card
```

To compile the FORTRAN program from cards the first statement card must be FTN,L,B and the last 3 cards must be END, END$, and a blank card. FTN is the designation that the FORTRAN compiler is to be used, L designates the cards are to be listed on the TTY, and B designates that a binary object tape is desired as an output from the compilation.

The FORTRAN deck of cards is compiled on the 2116B and the Hybrid System is operated in the following manner:

I. Turn the Main Power on:

The main computer power system ganged switch #5 in the upper right of the power rack is switched to 'ON'.

II. Turn the 2116B on:

A. The red power pushbutton (SYSTEM ON/OFF) on the upper right of the 2116B main frame is depressed - the red indicator light will come on indicating power has been applied to the main frame.

B. Push the square 'POWER' pushbutton on the 2116B control panel. The white light will come on.

C. On the 2116B mainframe, flip the paper tape photo reader toggle switch to 'ON'. The light in the reader will come one.

III. Turn the Teletype on. On the Teletype lower right side twist the LINE/OFF/LOCAL switch to the LINE position.

IV. Turn the Magnetic Tape System on. Open the window on the HP 3030 Mag Tape Unit. Mount an operative 'Hybrid System' Tape including the 'READ ring' (on the rear of the tape

reel) onto the right hand supply axle; turn the hub of the axle until the reel is seated tightly. Press the START/BRAKES Switch to the BRAKES position with one hand and thread the tape from the supply reel over the tape reading heads onto the take-up reel. Turn the take-up reel so that a few wraps of tape are buried. Press the START/BRAKES switch to the START position. Close the window. Press the 'LOAD POINT' button. The tape will move up to the load point and the LOAD POINT indicator will light. Press the 'AUTO' button and verify the system is in auto by noting that the yellow 'LOCAL' indicator goes out and the white 'AUTO' indicator comes on.

V. Bring the Mag Tape Unit on line: Using the Basic Binary Loader BBL load the paper tape labeled 'MTS BOOTSTRAP'. Place the tape under the Photoreader reading head with the paper tape feed holes toward the mainframe and push the little 'LOAD' tab on the tape reader up. On the 2116B control panel push the switch register toggle switches numbered 12 to 6 inclusive to the up position. All other switches should be down. Press the 'LOAD ADDRESS' button. Flip the 'Loader Enabled/Inhibited' toggle switch to the Enabled position. Press 'Preset' and 'Run'. The paper tape will be read in and will come to a halt. The T register should read 102077_8. Flip the 'Enabled/ Protected' toggle switch back to Protected and remove the paper tape from the optical reader by pushing the 'RUN'

tab down. Set the switch register toggle switch number 6 to the up position, all others down. Push the 'LOAD ADDRESS', 'PRESET' and 'RUN' buttons.

The TTY will print out 'HP MAGNETIC TAPE SYSTEM'
'*BATCH OPTION - DISABLED.'
'*SET ALL SWITCH REGISTER BITS TO ZERO (0).'
'NEXT?'

VI. Prepare the card reader:

On the rear of the optical card mark reader flip the toggle switch up to activate the reader. Lift the card weight from the hopper and place the FORTRAN deck with the cut corner forward face down into the hopper. Press "STOP" and "READY". The READY indicator should come on.

VII. Compile the FORTRAN program:

On the TTY type the following: ': PROG, FTN' then push RETURN and LINE FEED. The cards will be read into the digital computer from the card reader and the program will be typed onto the TTY one-by-one. After the program is compiled, the TTY will write out 'NO ERRORS', if there are no compiling errors; otherwise the cards must be changed and re-entered to correct the error. On the TTY Tape Punch push the 'ON' button and a compiled binary paper tape of the FORTRAN program will be punched.

After the paper tape has been punched, press the 'OFF' button and remove the paper tape from the TTY. The Mag Tape System will rewind and the TTY will print out 'NEXT?'

VIII. Load the binary tape into the digital computer:

Mount the paper tape on the photoreader as previously

described.

Type onto the TTY ':PROG, LOADR' and push 'RETURN' and 'LINE FEED'. The paper tape will be read and the TTY will type '*LOAD'. Set the switch register toggle switch #2 on the 2116B to the up position. Also set #15 up if a core memory map is not desired. Press 'Preset' and 'Run' on the 2116B. The 2116B will automatically transfer to core from the Mag Tape system any HP library routines, FORTRAN library routines required by the FORTRAN program and the Hybrid System Executive library. The TTY will print out 'LST'. If a memory address Listing is not desired, set switch #15 up and all others down. Otherwise, set all the switches down. Press 'Preset' and 'Run'. The TTY will print out '*RUN'. The Hybrid System Executive Library, FORTRAN program and all other routines required by the program are all in core.

IX. Turn the TR-48 on:

Turn the ANALOG/HYBRID Master Switch on the TR-48 to the ANALOG position. Turn the TR-48 on by pushing the 'POWER' pushbutton, and verify that the red light comes on.

X. Turn the DES-30 on:

On the DES-30 flip the toggle switch to ON and note that the 'POWER' indicator lights. Push 'Clear' and 'Run'. Set the DES-30 for the desired clocking by pushing the 1CPS, 1KCS, or 1 MCS button on the DES-30 mode control panel.

XI. Mate the systems for Hybrid Operation:

Mate the 2116B, TR-48, and DES-30 for Hybrid System Operation by turning the ANALOG/HYBRID Master Switch to HYBRID.

On the 2116B push 'Preset' and 'Run'. If the preceding FORTRAN example program is chosen the values of the first 10 pots and amps will be listed on the TTY and the 2116B will come to a halt.

The program has executed. Any variety of FORTRAN programs can be written using the Hybrid System Executive FORTRAN callable subroutines.

When the FORTRAN program execution is complete, deactivation of the Hybrid System may begin as follows:

1. Turn the ANALOG/HYBRID master switch to ANALOG.
2. Press the TR-48 'POWER' pushbutton and note that the red light goes off.
3. Turn the DES-30 toggle switch to the OFF position.
4. On the Mag Tape System, push the 'LOCAL' button and note that the yellow light comes on. Push the 'Rewind' button. When the tape comes to a halt, the 'Load Point' light will come ON. Depress 'Reverse' until the tape is off the take up reel. Open the window and press the 'BRAKES' button with one hand and spool all the tape onto the supply reel.
5. On the card reader, flip the toggle switch at the rear of the unit to the 'OFF' position.

6. On the TTY turn the LINE/OFF/LOCAL switch to the OFF position.
7. On the photoreader, flip the toggle switch to OFF.
8. On the 2116B control panel push the 'POWER' button and note that the light goes out.
9. Press the Red power pushbutton on the 2116B main frame and note that the red light does out.
10. On the power rack, flip the ganged power switch #5 down.

This completes a Hybrid System Run. For more complete details of the capability that is available via the FORTRAN subprograms see the Hybrid System Executive library routines listed on the preceding pages.

DIRECTIONS AND SUGGESTIONS FOR MODE CONTROL

When the system is operating in the Hybrid mode, the digital computer assumes control of the TR-48 and DES-30 modes according to the truth table (under Part I Mode Controk, Subroutine MODE (IBITS)) as a result of the user's software program or the Hybrid system executive software. There is one Exception:

In the Hybrid mode, if any of the OP, RST, CLR inputs become a logical one or the RUN input becomes a logical zero at the slave tray, control of the TR-48 and DES-30 is shifted from the digital computer to the DES-30 patch panel. In this way the TR-48 and DES-30 may be controlled as the result of a logic element output on the DES-30 or a comparator on the TR-48 patched through the trunk lines and the DES-30 patch panel. The big advantage to this control hierarchy is that the user need not patch a logic element or comparator output to one of the patchable logic sense lines, constantly test that sense line with the software in a loop and then initiate control of the TR-48 or DES-30 from the digital computer software - the control can be made directly from the DES-30 patch panel with a considerable savings in software and in time to initiate the action. An example of this technique follows: Suppose the system is in the HYBRID mode and the digital computer has controlled the TR-48 into the operate mode and the DES-30 into the run mode. The user specifies the analog solution to proceed until the output

of a certain amplifier reaches a specific voltage. The output of the amplifier can be wired to one of the TR-48 comparators where the voltage is compared to the specified voltage set into the comparator. When the threshhold voltage is reached, the comparator output will become a logical one. The comparator output is sent to the DES-30 over a trunk line. The trunk line termination on the DES-30 patch panel is patched to the RST bit and the CLR bit and the inversion patched to the RUN bit on the Slave Tray. When the amplifier voltage is reached, the TR-48 will take control from the digital computer and change the TR-48 mode from Operate to Reset and the DES-30 from Run to Clear.

Once the DES-30 OP, RST, RUN, and CLR inputs return to the 0010 state, control is returned to the 2116B. Re-entry into the FORTRAN program may be effected by testing the status of the OP, RST, RUN, and CLR outputs using the SENSE lines.

EXAMPLE OF PROGRAMMING THE REPEATED OPERATION (REPOP) MODE

The REPOP mode is a timed switching from the reset mode to the operate mode.

The REPOP mode can be programmed from the FORTRAN program in the following manner for a switching time of approximately 100 milliseconds to terminate after approximately one minute:

```
CALL TS
CALL RESET
DO 2 N=1, 300
```

```
      CALL TIMER
      CALL OP
      CALL TIMER
      CALL RESET
2     CONTINUE
```

The Time Scale Fast mode must first be called prior to the REPOP mode. The DVM input on the TR-48 should be grounded and the plotter should not be activated during the REPOP mode.

NOTES

I. On Programming

A. Care must be taken in programming the 2116B in FORTRAN as the sequence of execution may differ from the FORTRAN statements since the interrupt system is used for input and output. For example - FORTRAN WRITE statement may not be completed when the next successive statement is executed. The Assembly level routine ENDIO or the FORTRAN statement PAUSE will cause completion of the input or output before the next statement is executed.

B. The Hybrid System Executive Software assures that all Hybrid input and output functions are completed before control is returned to the FORTRAN program since the interrupt system is not used.

II. On DES-30 Clocking

Clocking is not provided on the DES-30 for the CONTROL Line outputs, and SENSE line, OP, RST, RUN or CLR inputs. If clocking is desired these inputs or outputs may be patched to the synchronous element gates (red inputs) on the DES-30 patch panel.

III. On TR-48 Internal Voltage Readings

Many of the voltages available at the selector switch on the TR-48 control panel and displayed on the Voltmeter during the analog mode are not available in the Hybrid mode.

IV. On the HOLD/SLAVE Mode

When the ANALOG/HYBRID switch is in the HYBRID mode the 2116B has control of the TR-48 through the DES-30.

The TR-48 is controlled manually by the TR-48 mode control panel push buttons when the ANALOG/HYBRID switch is in the ANALOG mode and the INT pushbutton is depressed.

However, the TR-48 is controlled by the DES-30 when the ANALOG/HYBRID switch is in the ANALOG position, the INT pushbutton is not depressed, and the HD/SL is depressed; this is called the slaved mode.

A. In both the HYBRID and Slaved mode, access to the Pot Set and Time Scale Fast TR-48 mode is available from the DES-30 patch panel as listed in Table 9 The Mode Control Hierarchy. This is different from the manufacturer's specification for the slaved mode.

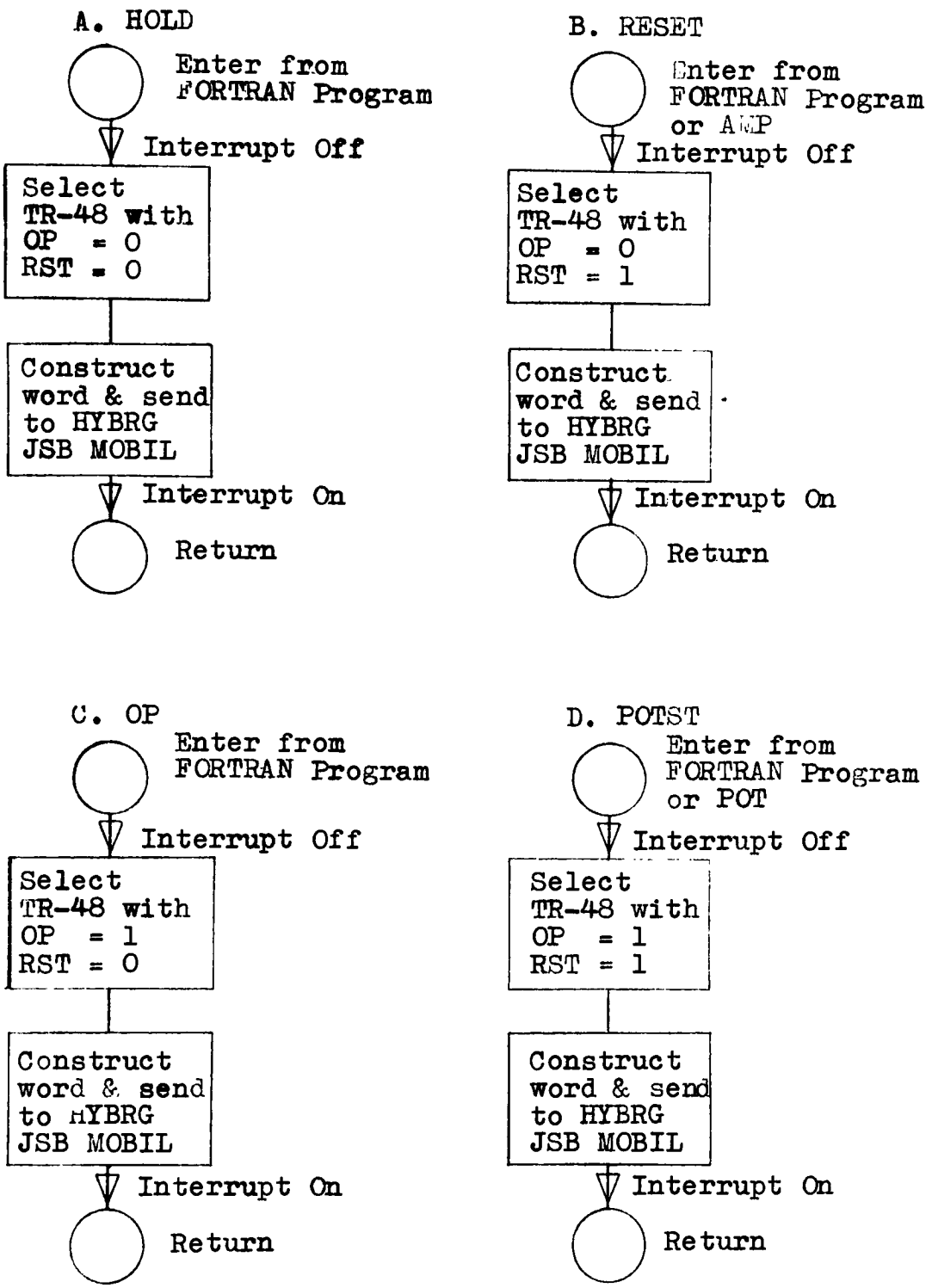
B. Automatic Control for operate and reset of an external plotter is available in the Analog mode and Hybrid mode, but is not available in the slaved mode. This is the same as the manufacturer's specification for the slaved mode.

VIII. HYBRID SYSTEM EXECUTIVE SOFTWARE

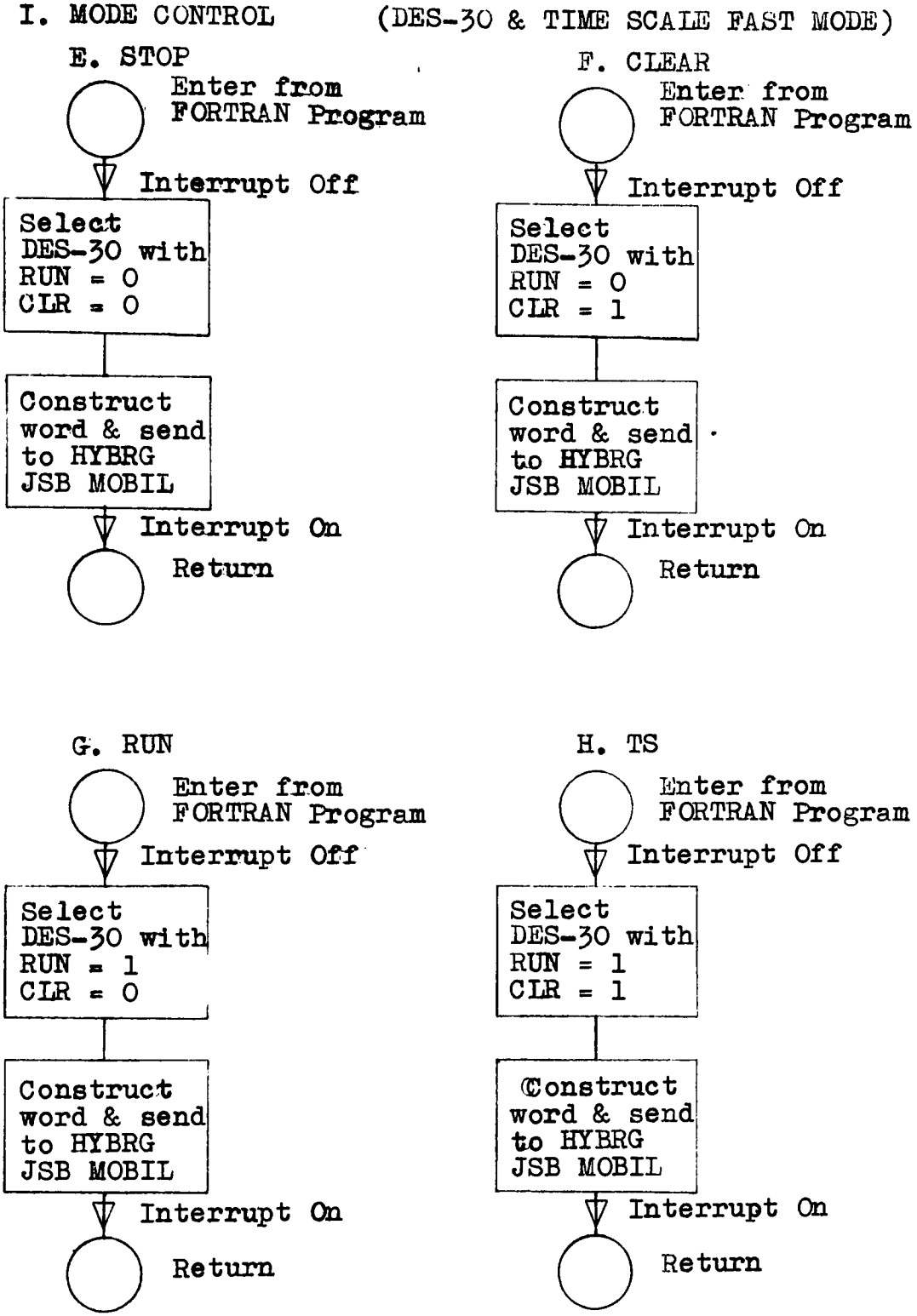
This section contains the flow chart Figure 11 and Assembly level listing for the Hybrid System Executive Software. The software provides the 2116B the sequential logic programming for the Mode Control, Potentiometer and Amplifier Reading, and the Hybrid Mode I/O Patchable Tray Control and Sense Lines.

The Hybrid System Executive Software is à totally self-sufficient software package requiring no external or library routines. Once the Hybrid System Executive Software is entered from the user's controlling main line program it cannot be interrupted until the hybrid function called has been completed and control returned to the main program.

Table 6, the ±16 bit duplex register Bit Assignments, may be helpful in following the flow chart and the Assembly level listing.

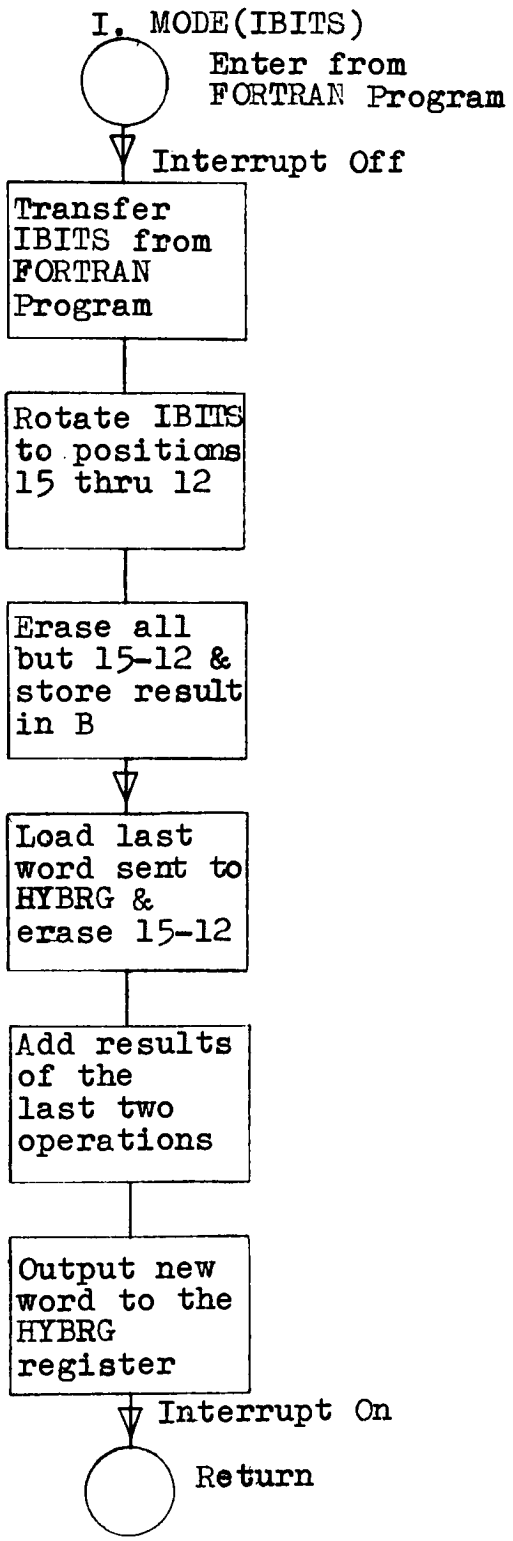


Hybrid System Executive Software Flow Chart
Figure 11 Sheet 1



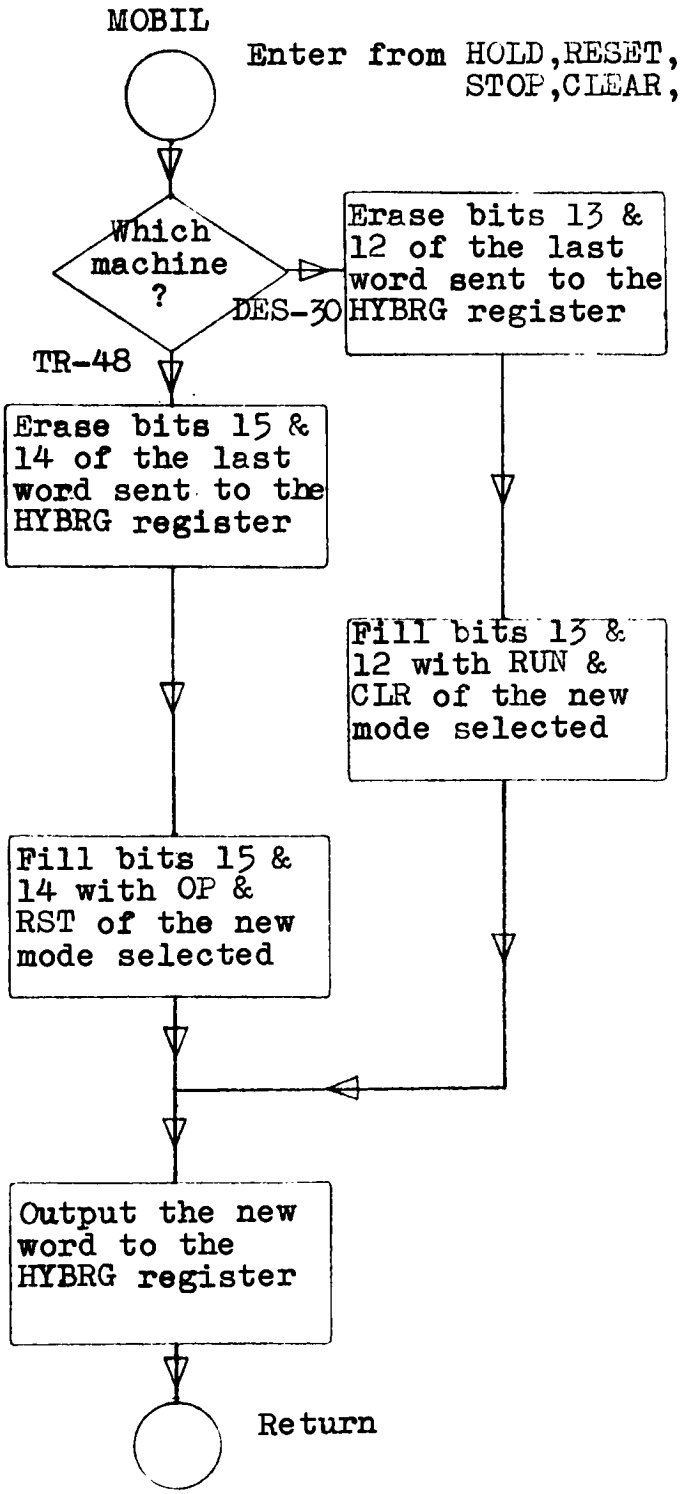
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 2

I. MODE CONTROL



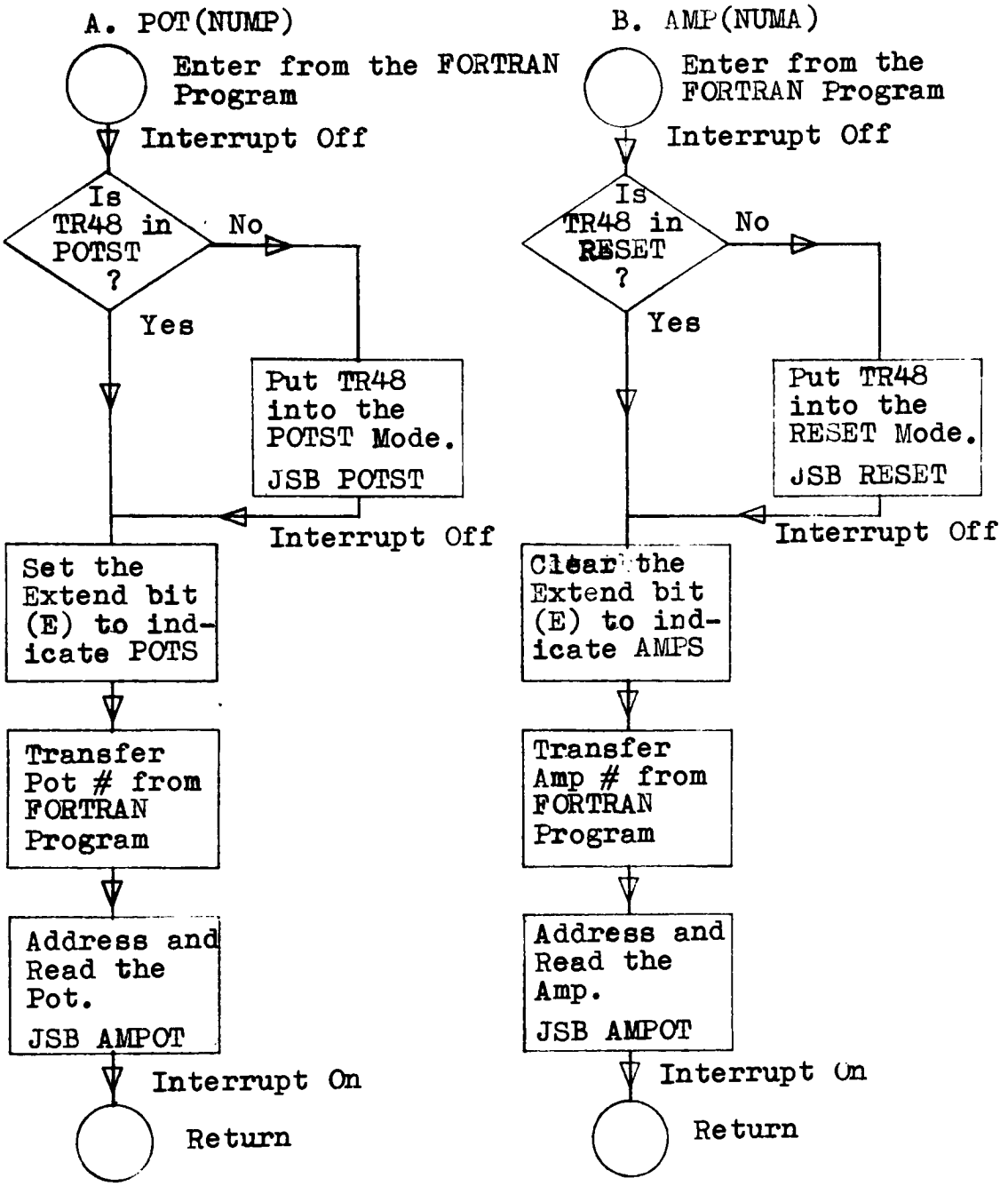
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 3

I. MODE CONTROL (SUBROUTINE MOBIL)



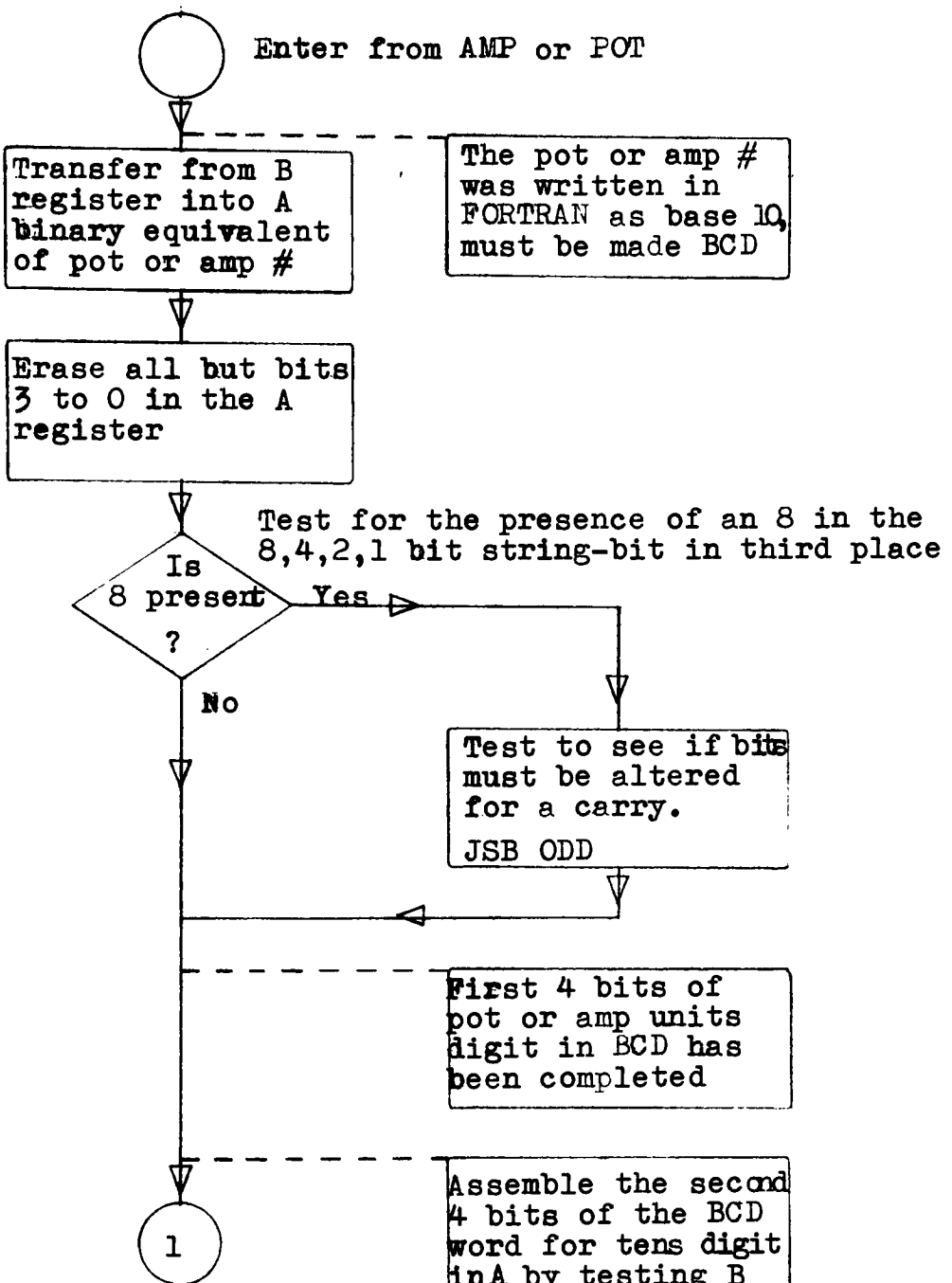
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 4

II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING



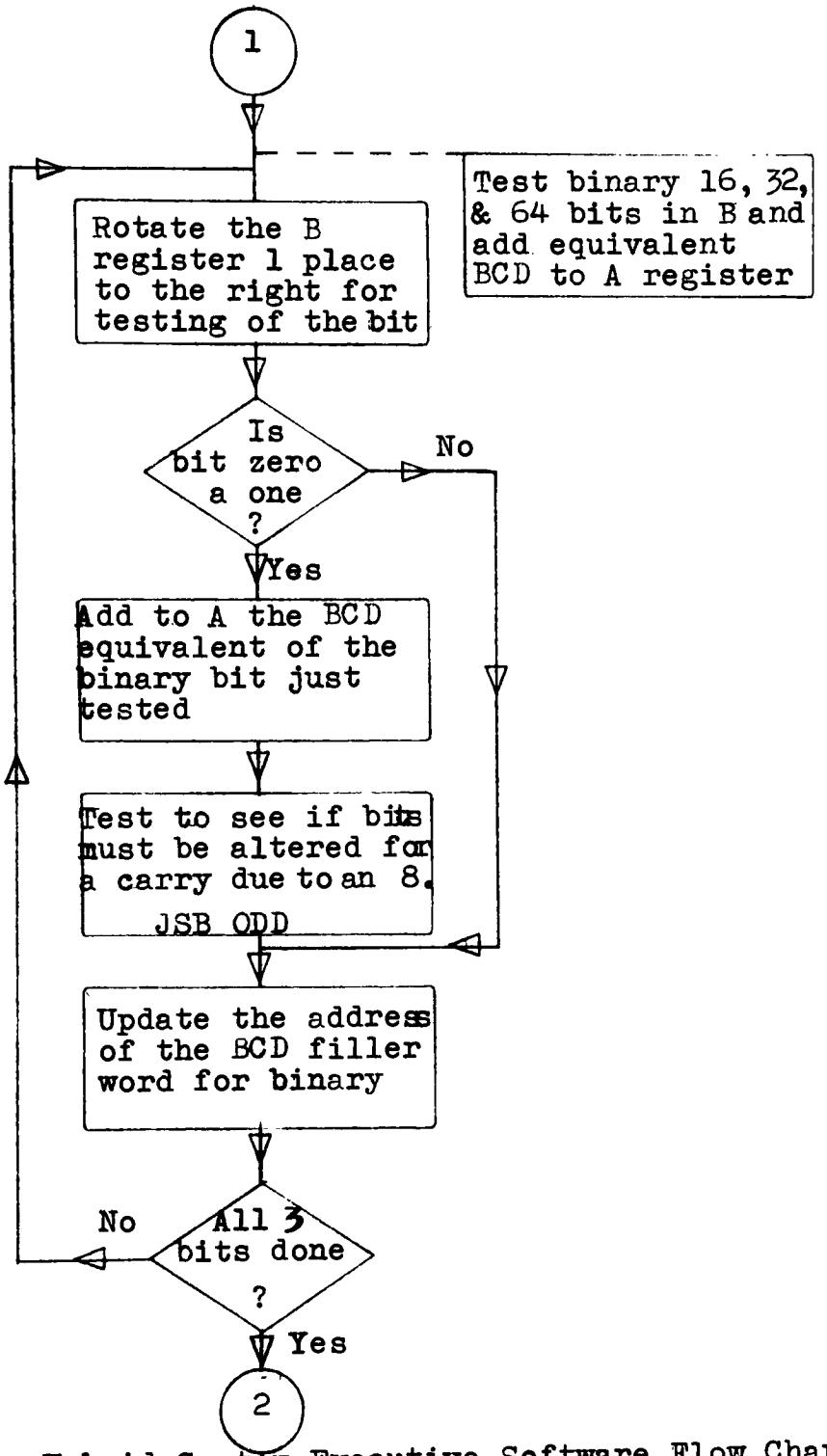
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 5

II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING
(SUBROUTINE AMPOT)



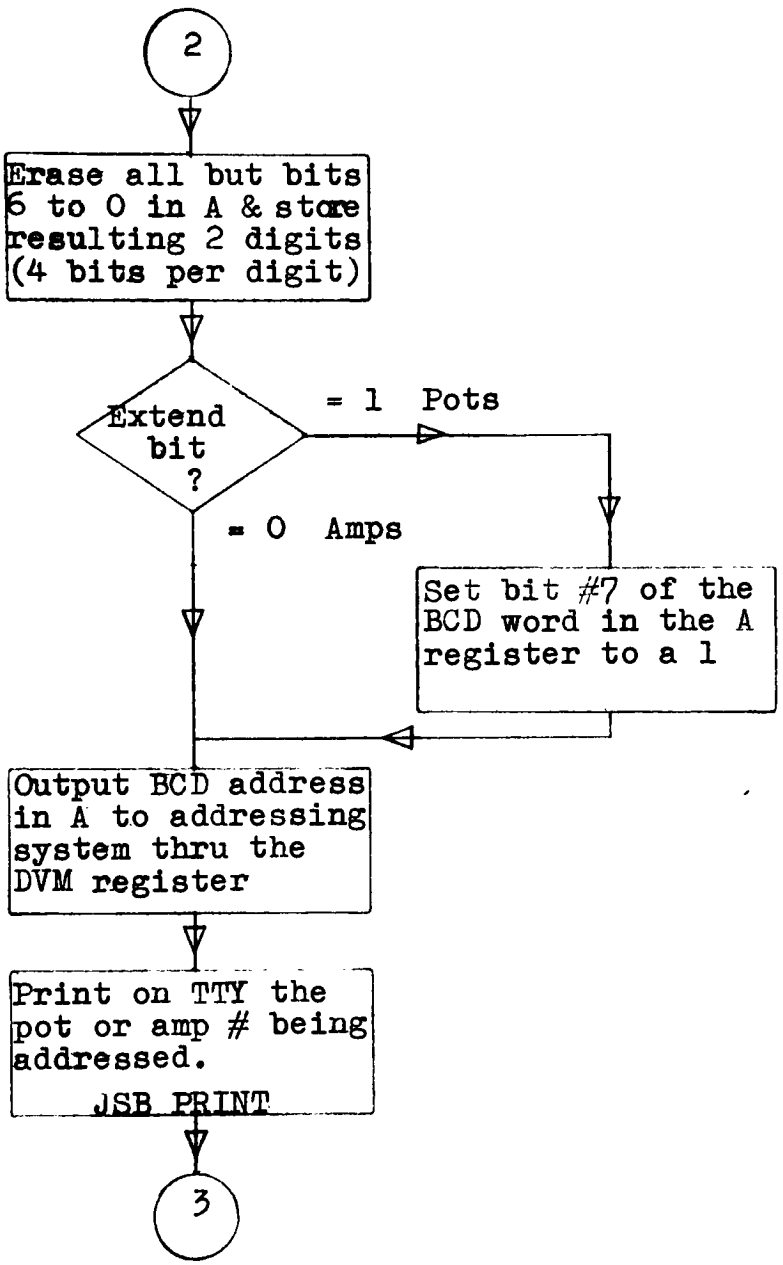
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 6

II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING (SUBROUTINE AMPOT)



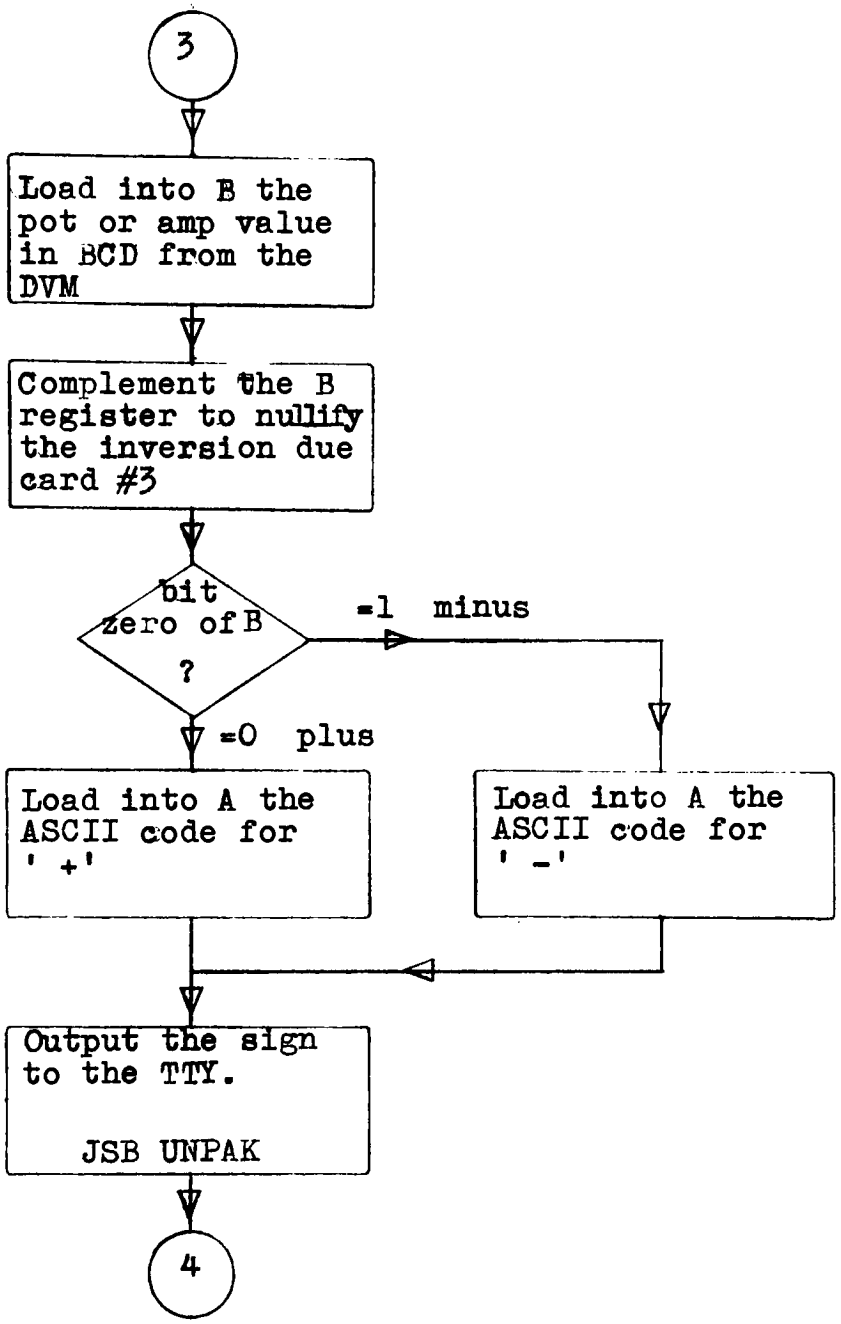
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 7

II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING (SUBROUTINE AMPOT)



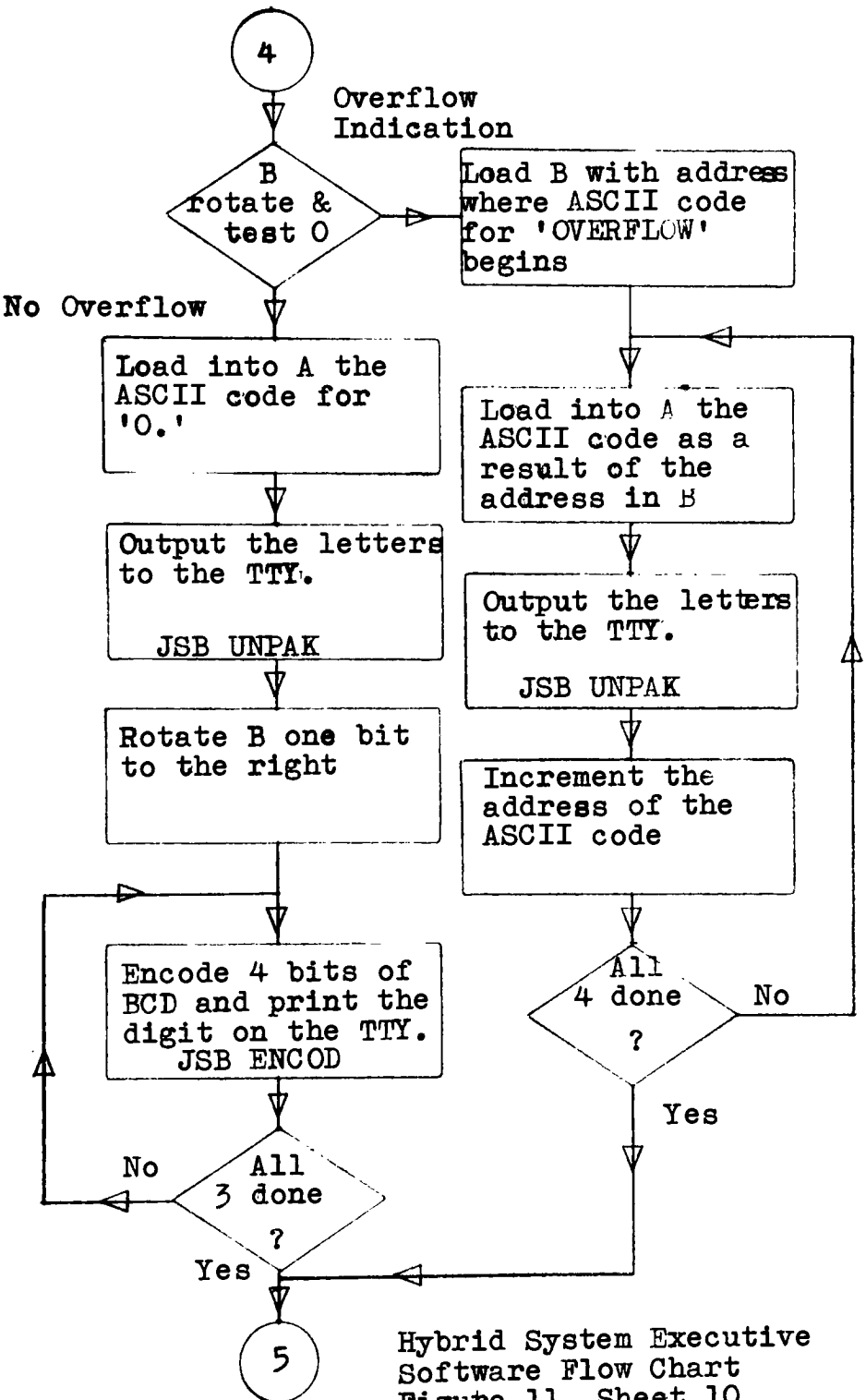
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 8

II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING (SUBROUTINE AMPOT)



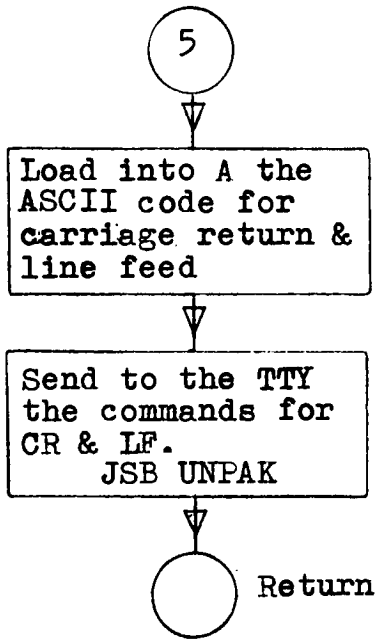
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 9

II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING (SUBROUTINE AMPOT)



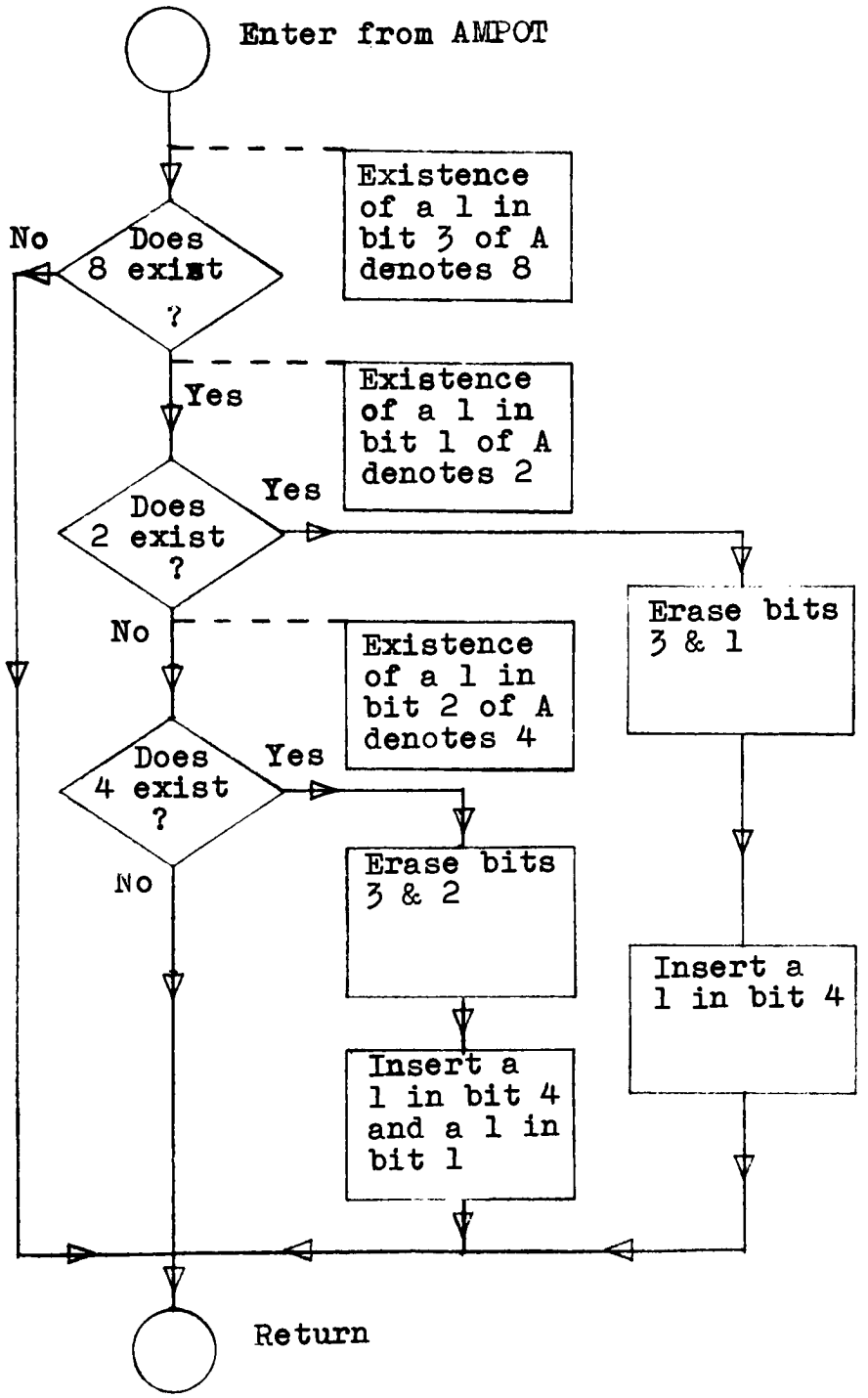
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 10

II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING (SUBROUTINE AMPOT)



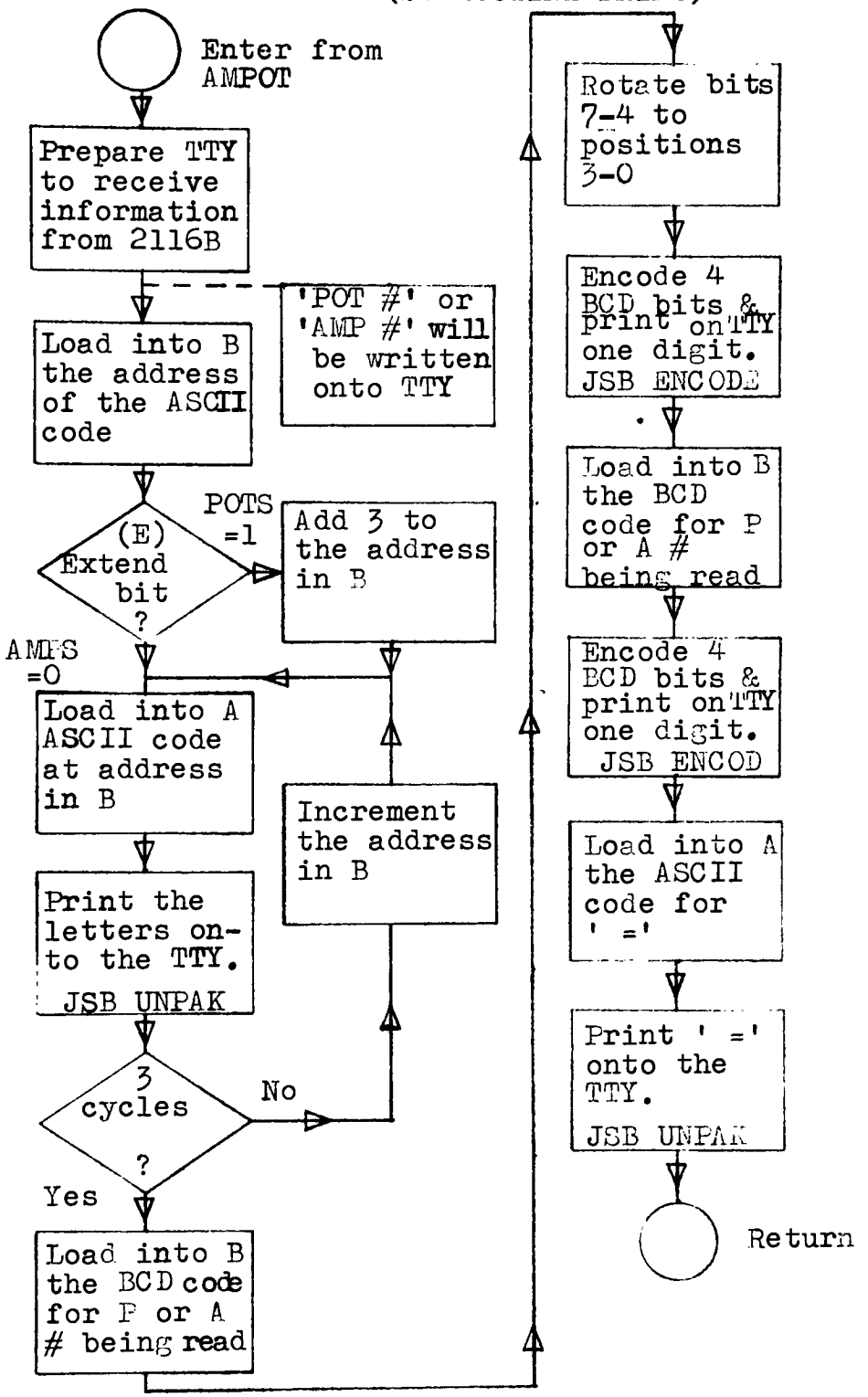
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 11

II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING (SUBROUTINE ODD)



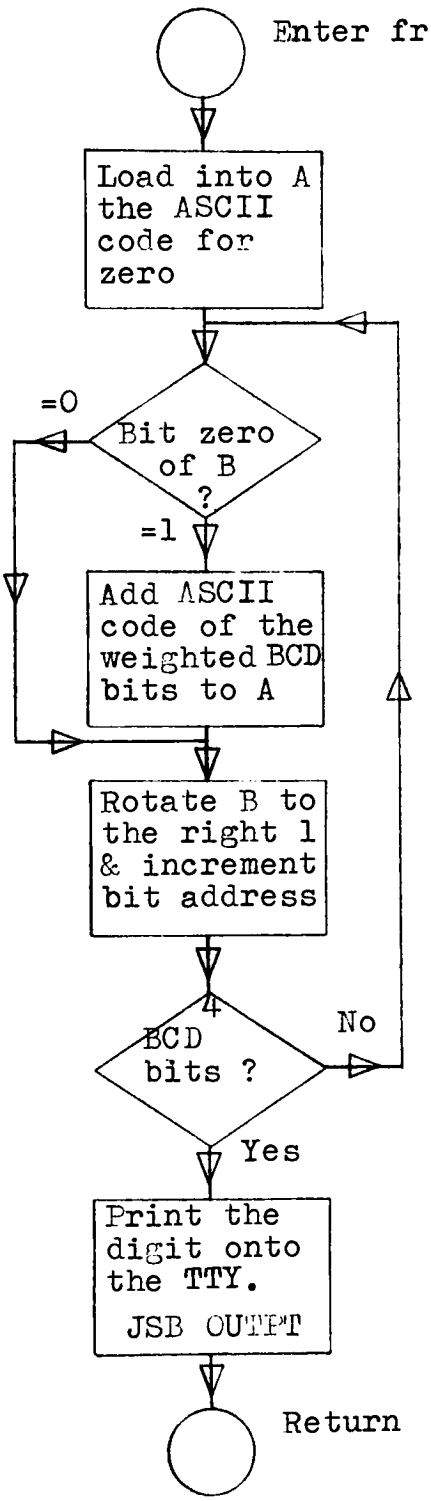
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 12

II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING
(SUBROUTINE PRINT)



Hybrid System Executive Software Flow Chart
Figure 11 Sheet 13

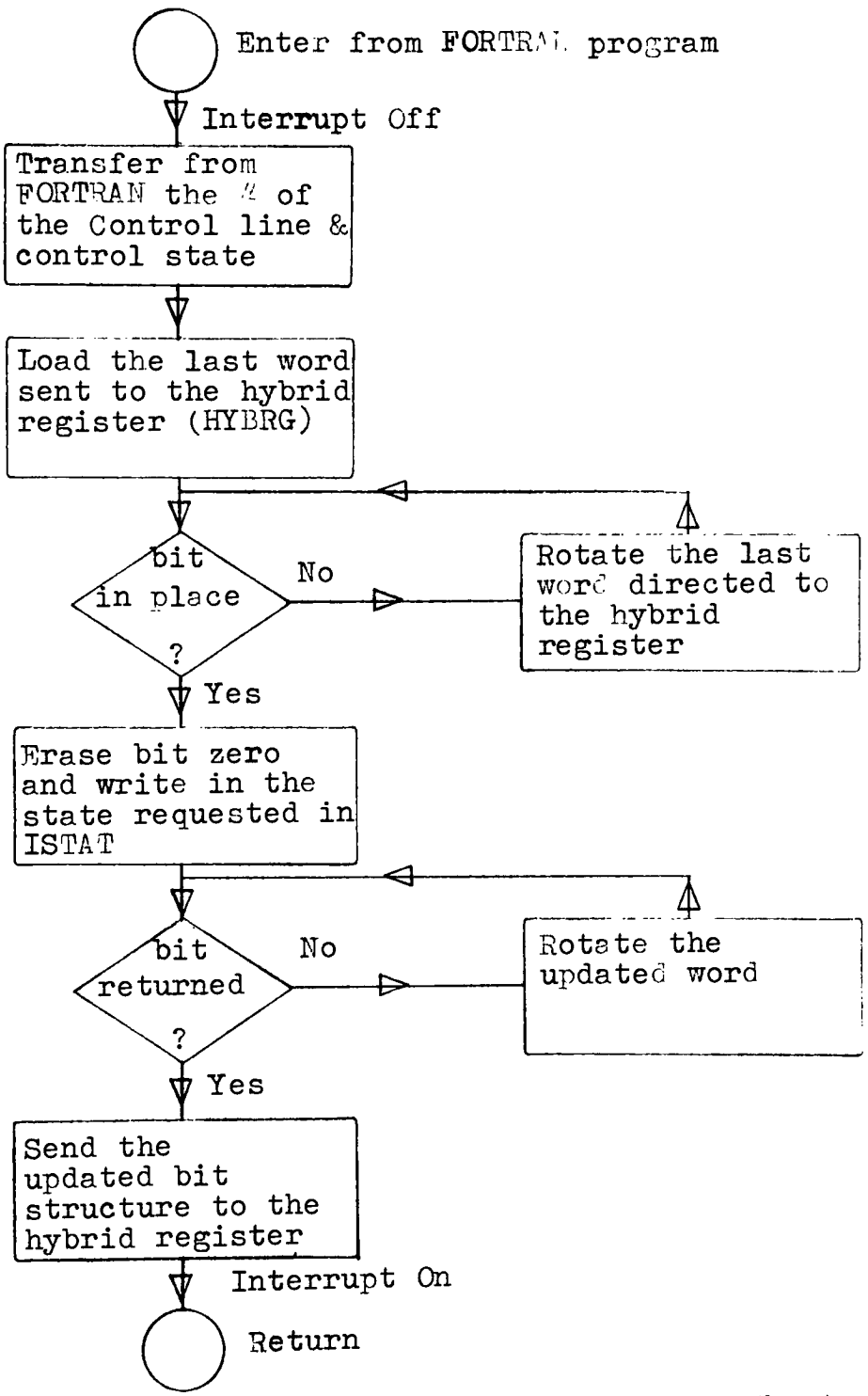
II. POTENTIOMETER AND AMPLIFIER ADDRESSING AND READING
(SUBROUTINE ENCOD)



Hybrid System Executive Software Flow Chart
Figure 11 Sheet 14

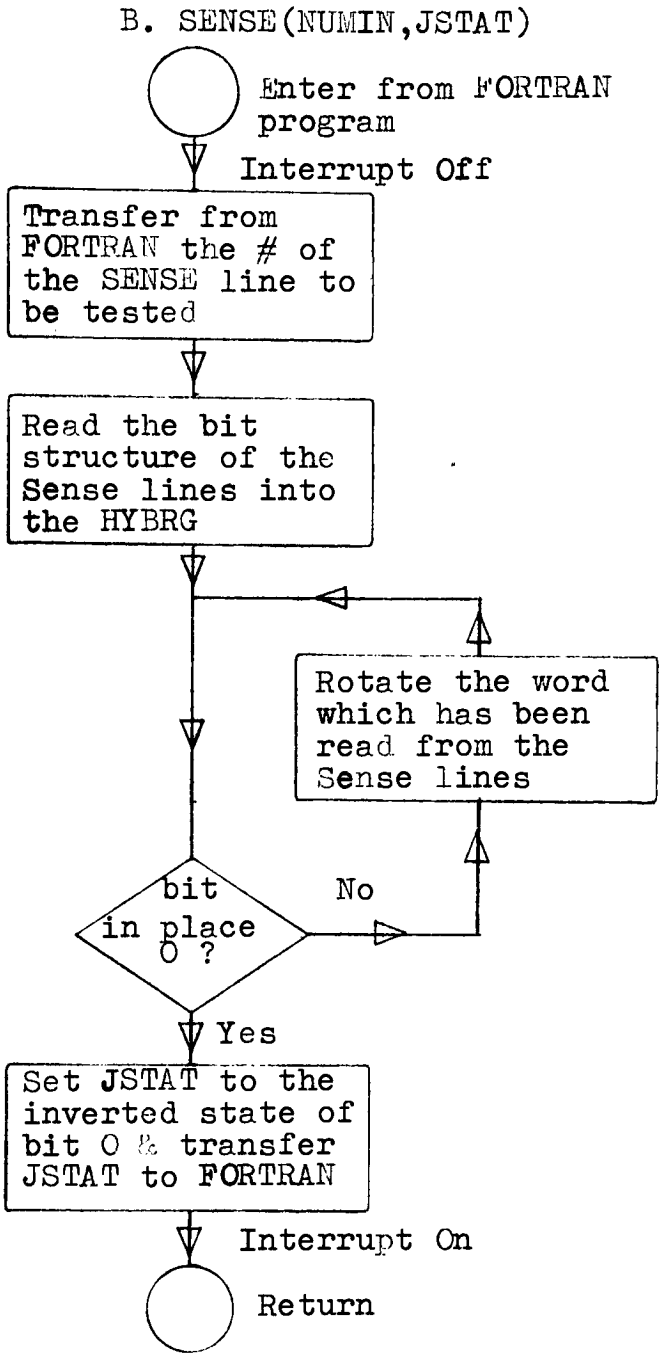
III. HYBRID MODE I/O PATCHABLE TRAY

A. CONT(NUMOT,ISTAT)



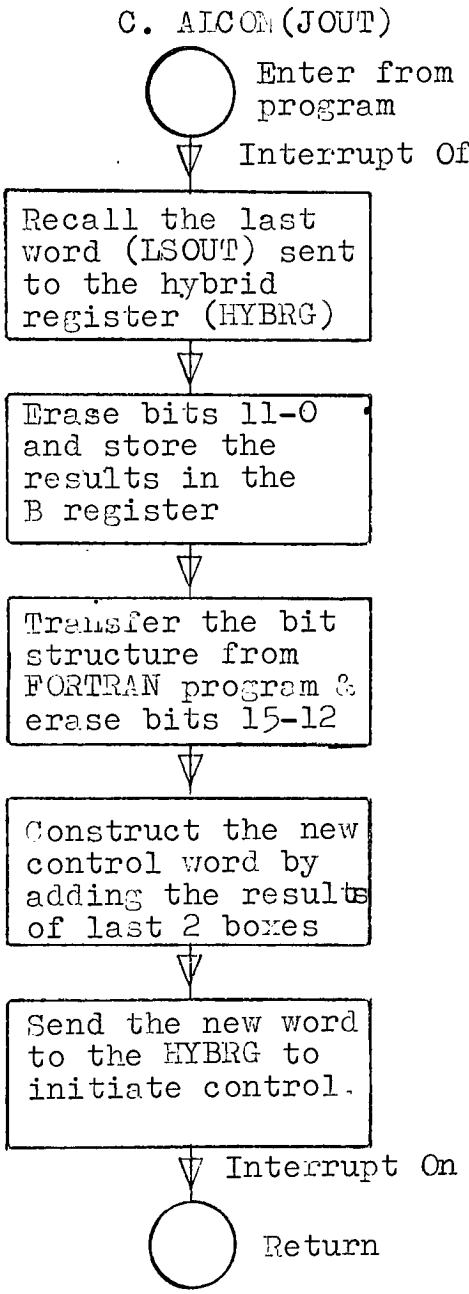
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 15

III. HYBRID MODE I/O PATCHABLE TRAY



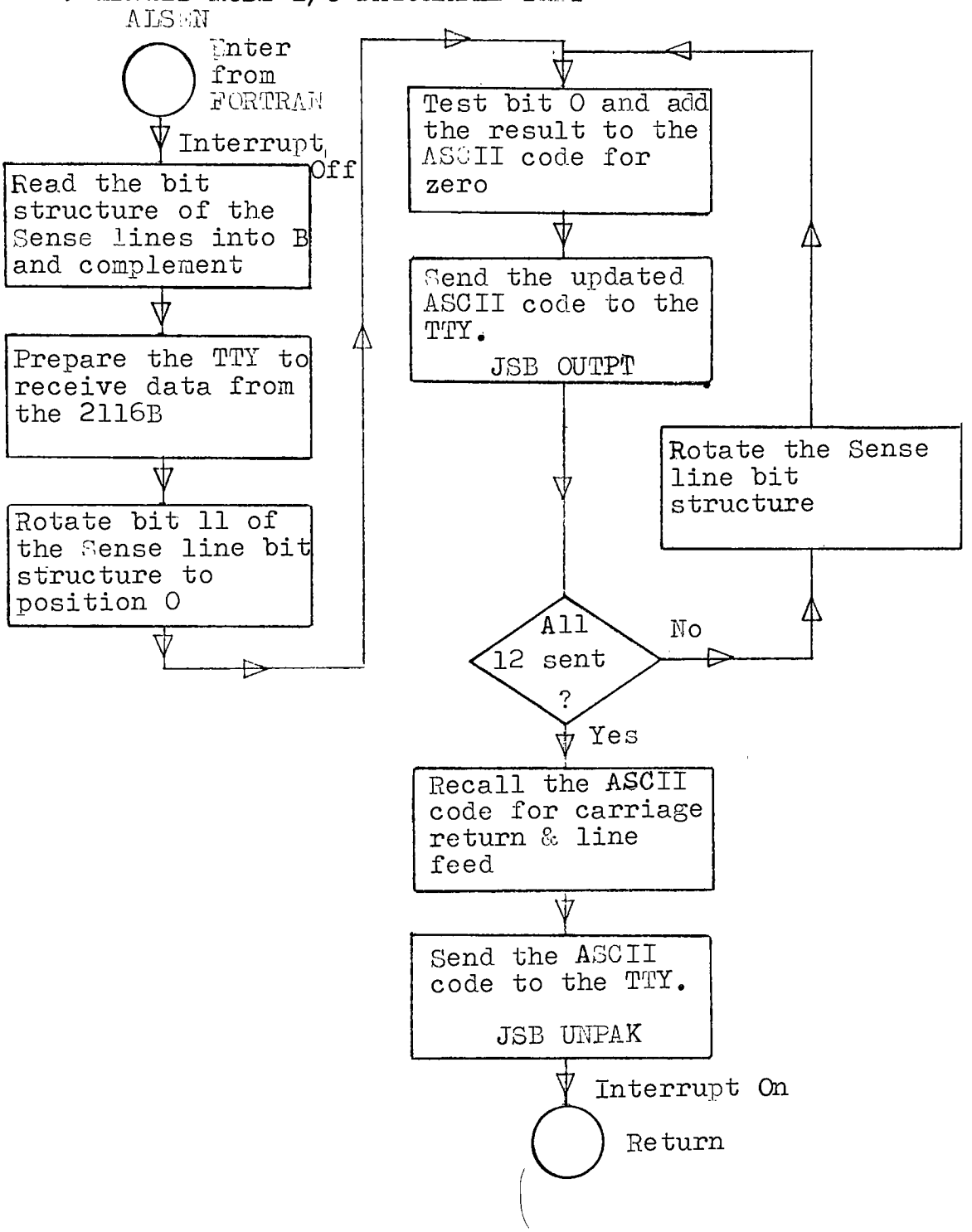
Hybrid System Executive Software Flow Chart
Figure 11 Sheet 16

III. HYBRID MODE I/O PATCHABLE TRAY

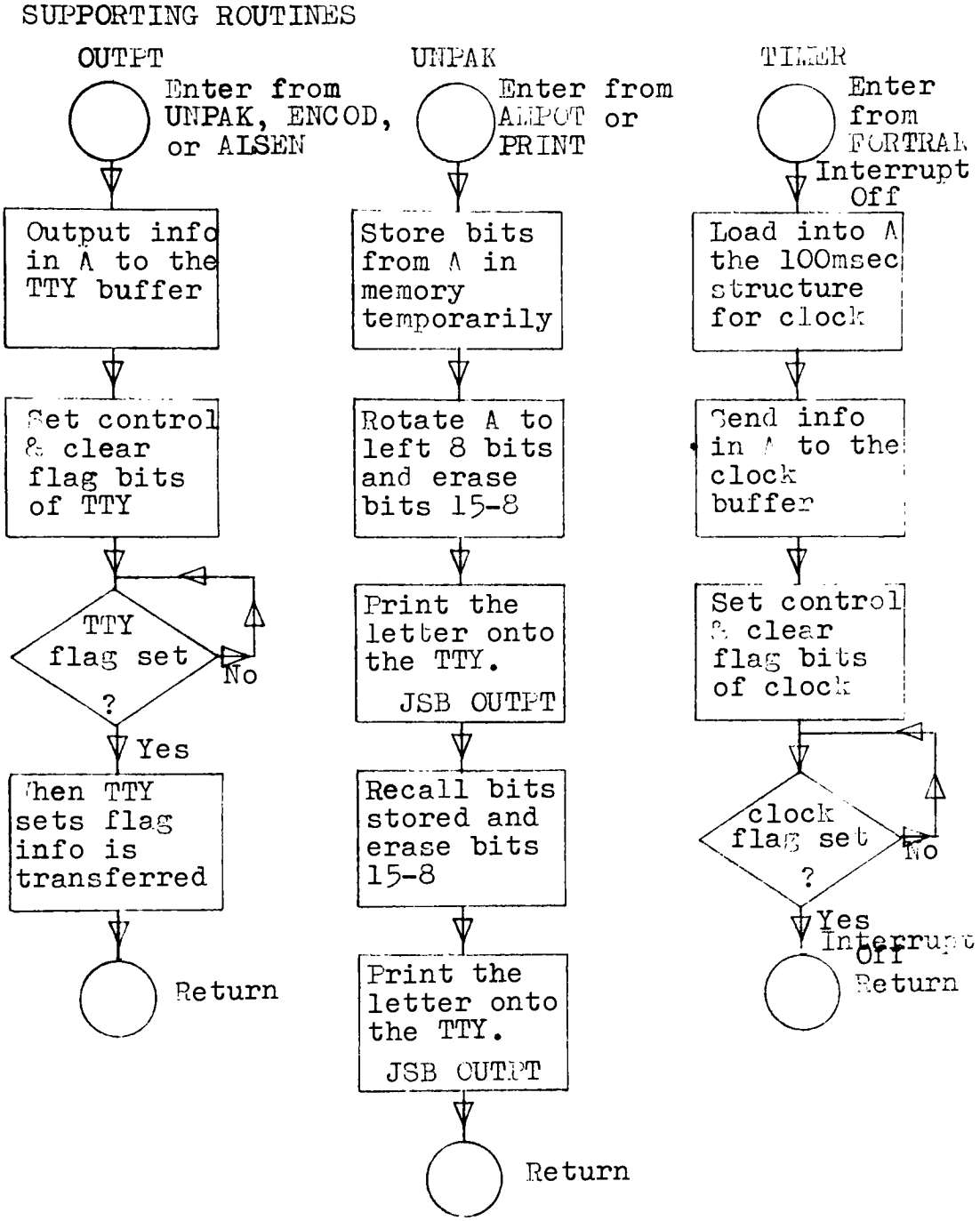


Hybrid System Executive Software Flow Chart
Figure 11 Sheet 17

III. HYBRID MODE I/O PATCHABLE TRAY



Hybrid System Executive Software Flow Chart
Figure 11 Sheet 18



Hybrid System Executive Software Flow Chart
Figure 11 Sheet 19

```
*HYBRID SYSTEM EXECUTIVE SOFTWARE
      NAM HYSYS
DVM   EQU 14B
HYBRG EQU 15B
CLOCK EQU 16B
TTY   EQU 20B
      ENT HOLD
HOLD  NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
*SET THE INDICATOR DESIGNATING THE TR48.
      CLA
*CLEAR B SINCE ZERO IS THE
*BIT STRUCTURE OF HOLD.
      CLB
*GO TO SUBROUTINE MOBIL FOR OPERATIONS
*ON THE A & B REGISTERS AND OUTPUT TO
*THE PARALLEL MODE CONTROL  UNIT.
      JSB MOBIL
      LDA HOLD,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP 0,I
      ENT RESET
RESET NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
*SET THE INDICATOR DESIGNATING THE TR48.
      CLA
*LOAD INTO B THE BIT
*STRUCTURE OF RESET
      LDB FIL01
*GO TO SUBROUTINE MOBIL FOR OPERATIONS
*ON THE A & B REGISTERS AND OUTPUT TO
*THE PARALLEL MODE CONTROL  UNIT.
      JSB MOBIL
      LDA RESET,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP 0,I
      ENT OP
OP    NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
*SET THE INDICATOR DESIGNATING THE TR48.
      CLA
*LOAD INTO B THE BIT
*STRUCTURE OF OPERATE
      LDB FIL10
```

```
*GO TO SUBROUTINE MOBIL FOR OPERATIONS
*ON THE A & B REGISTERS AND OUTPUT TO
*THE PARALLEL MODE CONTROL  UNIT.
      JSB MOBIL
      LDA OP,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP 0,I
      ENT POTST
POTST NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
*SET THE INDICATOR DESIGNATING THE TR48.
      CLA
*LOAD INTO B THE BIT
*STRUCTURE OF POTST.
      LDB FIL11
*GO TO SUBROUTINE MOBIL FOR OPERATIONS
*ON THE A & B REGISTERS AND OUTPUT TO
*THE PARALLEL MODE CONTROL  UNIT.
      JSB MOBIL
      LDA POTST,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP 0,I
      ENT STOP
STOP  NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
*SET THE INDICATOR DESIGNATING THE DES30
      CLA,INA
*CLEAR B SINCE ZERO IS THE
*BIT STRUCTURE OF STOP.
      CLB
*GO TO SUBROUTINE MOBIL FOR OPERATIONS
*ON THE A & B REGISTERS AND OUTPUT TO
*THE PARALLEL MODE CONTROL  UNIT.
      JSB MOBIL
      LDA STOP,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP 0,I
      ENT CLEAR
CLEAR NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
*SET THE INDICATOR DESIGNATING THE DES30
      CLA,INA
```

```
*LOAD INTO B THE BIT
*STRUCTURE OF CLEAR.
      LDB FIT01
*GO TO SUBROUTINE MOBIL FOR OPERATIONS
*ON THE A & B REGISTERS AND OUTPUT TO
*THE PARALLEL MODE CONTROL  UNIT.
      JSB MOBIL
      LDA CLEAR,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP 0,I
      ENT RUN
RUN   NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
*SET THE INDICATOR DESIGNATING THE DES30
      CLA,INA
*LOAD INTO B THE BIT
*STRUCTURE OF RUN.
      LDB FIT10
*GO TO SUBROUTINE MOBIL FOR OPERATIONS
*ON THE A & B REGISTERS AND OUTPUT TO
*THE PARALLEL MODE CONTROL  UNIT.
      JSB MOBIL
      LDA RUN,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP 0,I
      ENT TS
TS    NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
*SET THE INDICATOR DESIGNATING THE DES30
      CLA,INA
*LOAD INTO B THE BIT STRUCTURE OF THE
*TIME SCALE FAST MODE.
      LDB FIT11
*GO TO SUBROUTINE MOBIL FOR OPERATIONS
*ON THE A & B REGISTERS AND OUTPUT TO
*THE PARALLEL MODE CONTROL  UNIT.
      JSB MOBIL
      LDA TS,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP 0,I
      ENT MODE
MODE  NOP
*TURN THE INTERRUPT SYSTEM OFF.
```

```
       CLF 0
       LDA MODE,I
       STA WS4
*LOAD INTO A THE MODE CONTROL BIT
*STRUCTURE TRANSFERED FROM THE CALLING
*FORTRAN PROGRAM.
       ISZ MODE
       LDA MODE,I
       LDA 0,I
*ROTATE THIS WORD TO BITS 15-12.
       ALF,ALF
       ALF
*ERASE BITS 11-0 AND STORE THE RESULTS
*IN THE B REGISTER.
       AND MSKHY
       LDB 0
*LOAD INTO A THE LAST WORD SENT TO
*THE HYBRID REGISTER AND ERASE BITS 15-
*12 FROM LSOUT.
       LDA LSOUT
       AND MSKMO
*FILL IN THE NEW BITS 15-12 FROM B.
       ADA 1
*OUTPUT A TO THE HYBRID REGISTER BUFFER.
       OTA HYBRG
*STORE THE UPDATED BIT STRUCTURE OF THE
*HYBRG OUTPUT WORD.
       STA LSOUT
*TURN THE INTERRUPT SYSTEM ON.
       STF 0
*RETURN CONTROL TO THE FORTRAN CALLING
*PROGRAM.
       JMP WS4,I
MOBIL NOP
*ADD TO THE INDICATOR IN A THE POSITION
*OF THE BLANKING MASK.
       ADA MASKE
*LOAD THE BLANKING MASK INTO A.
       LDA 0,I
*THE BIT STRUCTURE OF THE LAST WORD
*DIRECTED TO THE HYBRID TRAY AND MODE
*CONTROL IS MASKED BY THE MASK ALREADY
*IN A. BITS 15 & 14 ARE BLANKED OUT IF
*THE TR48 MODE IS TO BE CONTROLLED;BITS
*13 & 12 ARE BLANKED OUT IF THE DES30 IS
*TO BE CONTROLLED.
       AND LSOUT
*ADD TO A THE COMPLEMENTED MODE BIT
*STRUCTURE IN B.
       ADA 1
*OUTPUT A TO THE HYBRID REGISTER BUFFER.
```

```
      OTA HYBRG
*STORE THE UPDATED BIT STRUCTURE OF THE
*HYBRG OUTPUT WORD.
      STA LSOUT
*RETURN CONTROL TO THE CALLING ASSEMBLER
*ROUTINE.
      JMP MOBIL,I
      ENT POT
POT   NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
      LDA LSOUT
*TEST THE LAST HYBRID REGISTER OUTPUT
*WORD TO SEE IF THE TR48 IS ALREADY IN
*THE POTSET MODE; IF IT IS CONTINUE; IF
*NOT, GO TO SUBROUTINE POTST.
*SET E INDICATING THAT A POT HAS BEEN
*SELECTED.
      RAL
      CCE,SLA,RSS
      JMP LONG
      RAL,SLA
      JMP ALLUP
*PUT THE TR48 INTO THE POT SET MODE.
LONG  JSB POTST
      DEF *+1
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
ALLUP LDA POT,I
      STA WS4
*LOAD INTO B THE # OF THE POT TO BE
*READ OUT.
      ISZ POT
      LDA POT,I
      LDB 0,I
*GO TO AMPOT, THE POT & AMP ADDRESSING &
*READING SUBROUTINE.
      JSB AMPOT
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP WS4,I
      ENT AMP
AMP   NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
      LDA LSOUT
*CLEAR E INDICATING THAT AN AMPLIFIER
*HAS BEEN SELECTED.
      RAL,CLE,SLA
*TEST THE LAST HYBRID REGISTER OUTPUT
```

```
*WORD TO SEE IF THE TR48 IS ALREADY IN
*THE RESET MODE; IF IT IS CONTINUE; IF
*NOT GO TO RESET.
       JMP LENG
       RAL,SLA
       JMP ALLOK
*PUT THE TR48 INTO THE RESET MODE.
LENG   JSB RESET
       DEF *+1
*TURN THE INTERRUPT SYSTEM OFF.
       CLF 0
ALLOK LDA AMP,I
       STA WS4
*LOAD INTO B THE # OF THE AMPLIFIER TO
*BE READ OUT.
       ISZ AMP
       LDA AMP,I
       LDB 0,I
*GO TO AMPOT, THE POT & AMP ADDRESSING
*AND READING SUBROUTINE.
       JSB AMPOT
*TURN THE INTERRUPT SYSTEM ON.
       STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
       JMP WS4,I
AMPOT NOP
*DECODE B THE # OF THE POT OR AMP TO BE
*ADDRESSED FROM BINARY TO BCD.
*CONVT IS THE ADDRESS OF THE FIRST BCD
*FILLER WORD CONS1, LOAD CONVT INTO
*WORKING STORAGE #1 TO BE INDEXED LATER.
       LDA CONVT
       STA WS1
*LOAD INTO WORKING STORAGE #2 THE NEGAT-
*IVE OF THE # OF EACH BCD DIGIT(3 DIGIT)
       LDA NEG3
       STA WS2
*LOAD INTO A THE POT OR AMP BINARY # AND
*ERASE ALL BUT BITS 3-0.
       LDA 1
       AND MSK4
*TEST BIT 2 OF B, IF BIT 2 IS A 1, GO TO
*ODD.
       RBR,RBR
       RBR,SLB
*ODD IS A SUBROUTINE TO TEST FOR THE
*PRESENCE OF AN 8 IN THE BCD 8,4,2,1 BIT
*STRING.
       JSB ODD
BITS   RBR
       SLB,RSS
```

```
*TEST BIT 3 OF B, IF IT IS A 1, ADD
*CONS1 TO A AND GO TO ODD. IF BIT 3 IS
*A 0 CONTINUE.
      JMP *+3
      ADA WS1,I
      JSB ODD
*INDEX WS1 TO THE ADDRESS OF THE NEXT
*BCD FILLER WORD.
      ISZ WS1
      ISZ WS2
*IF 3 PASSES HAVE BEEN MADE, CONTINUE,
*IF NOT, GO TO BITS FOR MORE DECODING.
      JMP BITS
*ERASE ALL BUT BITS 6-0.
      AND MSK7
*STORE THE BIT STRUCTURE IN BCD OF THE
*POT OF AMP # DECODED FROM BINARY.
      STA BCD
*IF THE E IS SET, INDICATING A POT, SET
*BIT 7 OF THE ADDRESS TO A 1.
      SEZ
      ADA FIL7
*OUTPUT THE BCD BIT STRUCTURE IN A TO
*THE DIODE MATRICES IN THE TR48 FOR
*ADDRESSING THE POT OR AMP SPECIFIED.
      OTA DVM
*WHILE WAITING FOR THE ADDRESSING
*RELAYS TO FLIP, GO TO SUBROUTINE PRINT
*TO WRITE OUT ON THE TTY THE POT OR AMP
*NUMBER BEING ADDRESSED.
      JSB PRINT
*READ FROM THE DVM THE VALUE OF THE POT
*OR AMP IN BCD, AND LOAD INTO B.
      STC DVM,C
      SFS DVM
      JMP *-1
      LIB DVM
      CLC DVM,C
*COMPLEMENT B SINCE THE HARDWARE ON CARD
*#3 IN THE TR48 USED FOR POWER BUFFERING
*COMPLEMENTED THE ORIGINAL BCD VALUE
*READ FROM THE DVM OUTPUT.
      CMB,SLB
*TEST THE BIT 0 OF THE VALUE WORD, IF IT
*IS A 0, THE VALUE IS POSITIVE, IF IT IS
*A 1 THE VALUE IS NEGATIVE.
      JMP *+3
      LDA PLUS
      JMP *+2
      LDA MINUS
*WRITE OUT ON THE TTY WHETHER THE VALUE
```

```
*IS POSITIVE OF NEGATIVE.
       JSB UNPAK
       RBR
       SLB,RSS
*TEST BIT #1 OF THE VALUE; IF IT IS A 0
*GO TO DECOD. IF IT IS A 1, THE VALUE OF
*THE POT OR AMP BEING READ IS 10.00
*VOLTS(ONE MACHINE UNIT) OR GREATER,
*THEREFORE WRITE ON THE TTY THE WORD
*'OVERFLOW', AND BEGIN TERMINATION OF
*THE POT OR AMP READ CYCLE BY GOING TO
*CONK FOR CARRIAGE RETURN AND LINE FEED
*ON THE TTY.
       JMP DECOD
       LDA NEG4
       STA WS1
       LDB FULL
       LDA 1,I
       JSB UNPAK
       INB
       ISZ WS1
       JMP *-4
       JMP CONK
*IF BIT 1 OF THE VALUE WORD WAS NOT A 1,
*INDICATING OVERFLOW, THE VALUE BEGINS
*WITH '0.'; WRITE THIS ON THE TTY.
DECOD LDA OWEPT
       JSB UNPAK
ROT    RBR
*LOAD INTO WORKING STORAGE #3 THE
*NEGATIVE OF THE REMAINING # OF DIGITS
*OF THE VALUE TO BE SENT TO THE
*TTY, THE TOTAL NUMBER OF DIGITS IS 3.
       LDA NEG3
       STA WS3
*ENCODE THE VALUE WORD TO THE ASCII CODE
*REPRESENTATIVE OF THE DIGITS READ FROM
*THE DVM.
       JSB ENCOD
       ISZ WS3
       JMP *-2
*LOAD INTO A THE ASCII CODE FOR CARRIAGE
*RETURN LINE FEED AND OUTPUT IT TO THE
*TTY.
CONK   LDA CRLF
       JSB UNPAK
*RETURN CONTROL THRU POT OR AMP TO THE
*FORTRAN CALLING ROUTINE.
       JMP AMPOT,I
*THIS ROUTINE TESTS WHETHER AN 8 IN THE
*8,4,2,1 BCD STRING IS PRESENT, SINCE
```

```
*THE SIMULTANEOUS OCCURANCE OF AN 8 & A
*4 OR AN 8 & A 2 OF A BCD WORD ADD TO
*THE NEXT LEFT BCD DIGIT.
ODD   NOP
      RAR,RAR
      RAR,SLA
      JMP *+3
*AN EIGHT IS PRESENT, SO TEST TO SEE IF
*A 2 ALSO EXISTS.
      ALF,RAR
      JMP ODD,I
      RAL,RAL
      SLA
      JMP B002
*AN 8 AND A 2 EXIST SIMULTANEOUSLY, SO
*ERASE THEM, AND WRITE IN A 10.
      RAR,SLA,RAL
      JMP B004
*AN 8 AND A 4 EXIST SIMULTANEOUSLY, SO
*ERASE THEM, AND WRITE IN A 10 AND A 2.
ENODD RAL
      JMP ODD,I
B002  AND MSK82
      ADA TEN
      JMP ENODD
B004  AND MSK84
      ADA FIL84
      JMP ENODD
PRINT NOP
*SET THE CONTROL ON THE TTY TO EXPECT AN
*OUTPUT FROM THE 2116B.
      LDA KNTRL
      JSB OUTPT
*THE # OF PACKED ASCII WORDS FOR 'AMP #'
*OR 'POT #' IS THREE, SO A -3 IS STORED
*IN WS1 FOR INDEXING.
      LDA NEG3
      STA WS1
*SHOW IS THE STARTING ADDRESS OF THE
*ASCII CODE FOR 'AMP #'.
      LDB SHOW
*TEST E, IF E IS 1, POTS ARE INDICATED,
*SO ADD 3 TO THE LOCATION SHOW, WHICH
*IS THE LOCATION OF 'POT #' IN ASCII.
      SEZ
      ADB POS3
STILL LDA 1,I
*WRITE 'AMP #' OR 'POT #' ON THE TTY.
      JSB UNPAK
      INB
      ISZ WS1
```

```
      JMP STILL
*LOAD INTO B THE # IN BCD OF THE POT OR
*AMP REQUESTED.
      LDB BCD
      BLF,BLF
      BLF

*AND WRITE IT OUT ON THE TTY.
      JSB ENCOD
      LDB BCD
*ENCODE THE POT OR AMP NUMBER UNITS
*DIGIT.
      JSB ENCOD
*LOAD INTO A THE PACKED ASCII CODE FOR
*' =' AND WRITE IT OUT ON THE TTY.
      LDA BLKEQ
      JSB UNPAK
*RETURN CONTROL TO THE CALLING SPOT
*WHERE THE POT OR AMP VALUE IS TO BE
*READ IN FROM THE DVM.
      JMP PRINT,I
ENCOD NOP
*LOAD INTO A -4, THE NEGATIVE OF THE #
*OF BITS IN A BCD DIGIT (8,4,2,1) AND
*STORE IN WS1.
      LDA NEG4
      STA WS1
*LOAD INTO A THE STARTING POINT OF THE
*WEIGHTING TO BE ADDED TO THE ASKII CODE
*AND STORE IT IN WS2.
      LDA ADDSS
      STA WS2
*ADD TO A THE ASCII CODE FOR ZERO.
      LDA ANS
NODIG SLB
*TEST THE 4 BCD BITS SEQUENTIALLY AND
*ACCUMULATE THE WEIGHTING OF THE BITS
*1,2,4,8  IN WS2 TO BE SENT IN ASCII
*TO THE TTY AFTER ALL FOUR BITS ARE READ
*OUTPUT A TO THE TTY BUFFER.
      ADA WS2,I
      RBR
      ISZ WS2
      ISZ WS1
      JMP NODIG
      JSB OUTPT
      JMP ENCOD,I
OUTPT NOP
      OTA TTY
*SET THE CONTROL AND CLEAR THE FLAG BITS
*OF THE TTY REGISTER.
```

```
      STC TTY,C
*WAIT UNTIL THE TTY SETS THE FLAG, INDI-
*CATING A DATA TRANSFER HAS BEEN MADE.
      SFS TTY
      JMP *-1
      CLC TTY
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP OUTPT,I
UNPAK NOP
*SINCE THERE ARE TWO 8 BIT ASCII LETTERS
*PACKED INTO A 16 BIT WORD, BITS 15-8
*ARE FIRST ROTATED TO POSITIONS 7-0.
*BITS 15-8 ARE THEN ERASED AND CONTROL
*IS SHIFTED TO THE OUTPT SUBROUTINE
*TO OUTPUT THE FIRST LETTER TO THE TTY.
      STA TEMPA
      ALF,ALF
      AND MASK
      JSB OUTPT
*THE ORIGINAL WORD IS RETRIEVED FROM
*TEMPORARY STORAGE.
      LDA TEMPA
*BITS 15-8 ARE THEN ERASED AND CONTROL
*IS SHIFTED TO THE OUTPT SUBROUTINE TO
*OUTPUT THE SECOND LETTER TO THE TTY.
      AND MASK
      JSB OUTPT
*RETURN CONTROL TO THE CALLING PROGRAM.
      JMP UNPAK,I
      ENT TIMER
TIMER NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
*LOAD INTO A THE BIT STRUCTURE OF THE
*TIME DESIGNATED TO BE COUNTED ON THE
*CRYSTAL CLOCK, AND OUTPUT THE VALUE TO
*THE CLOCK BUFFER.
      LDA POS3
      OTA CLOCK
*SET THE CONTROL AND CLEAR THE FLAG BITS
*OF THE CLOCK REGISTER.
      STC CLOCK,C
*WAIT UNTIL THE CLOCK SETS THE FLAG
*INDICATING THE END OF THE TIME COUNTED.
      SFS CLOCK
      JMP *-1
*CLEAR THE CONTROL BIT OF THE CLOCK
*REGISTER.
      CLC CLOCK
      LDA TIMER,I
*TURN THE INTERRUPT SYSTEM ON.
```

```
       STF 0
*RETURN CONTROL TO THE CALLING PROGRAM.
       JMP 0,I
       ENT CONT
CONT   NOP
*TURN THE INTERRUPT SYSTEM OFF.
       CLF 0
       LDA CONT,I
       STA WS4
*TRANSFER FROM THE FORTRAN PROGRAM THE
*NUMBER OF THE BIT TO BE CHANGED AND THE
*STATE TO WHICH IT IS TO BE CHANGED.
*LOAD THEM INTO A & B RESPECTIVELY.
       ISZ CONT
       LDA CONT,I
       LDA 0,I
       ISZ CONT
       LDB CONT,I
       LDB 1,I
*CHANGE THE BIT # INTO A NEGATIVE NUMBER
*TO BE INDEXED BY ISZ AND STORE IN WS1
*AND WS2.
       CMA
       STA WS1
       STA WS2
*LOAD INTO A THE BIT STRUCTURE THAT WAS
*LAST DIRECTED TO THE HYBRID TRAY AND
*MODE CONTROL.
       LDA LSOUT
*ROTATE LAST WORD OUT UNTIL THE POSITION
*OF THE DESIGNATED BIT IS REACHED.
SPIN   ISZ WS1
       JMP *+2
       JMP SLAP
       RAR
       JMP SPIN
*BLANK THAT BIT OUT OF THE WORD AND
*WRITE IN A ONE IF ISTAT IN B WAS
*DESIGNATED A ONE, OTHERWISE LEAVE IT
*BLANK.
SLAP   AND MSK0
       SLB
       INA
NIPS   ISZ WS2
       JMP *+2
       JMP FINAL
       RAL
*ROTATE THE BITS BACK TO THEIR ORIGINAL
*POSITIONS.
       JMP NIPS
*OUTPUT A TO THE HYBRID REGISTER BUFFER.
```

```
FINAL OTA HYBRG
*STORE THE UPDATED BIT STRUCTURE OF THE
*HYBRG OUTPUT WORD.
      STA LSOUT
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*CONTROL OF THE PROGRAM IS RETURNED TO
*THE FORTRAN CALLING PROGRAM.
      JMP WS4,I
      ENT SENSE
SENSE NOP
*TURN THE INTERRUPT SYSTEM OFF.
      CLF 0
      LDA SENSE,I
      STA WS4
*TRANSFER FROM THE FORTRAN PROGRAM THE
*NUMBER OF THE BIT TO BE READ FROM THE
*HYBRID TRAY AND LOAD IT INTO A.
      ISZ SENSE
      LDA SENSE,I
      LDA 0,I
*NEGATE THE BIT # TO BE INDEXED BY ISZ
*AND STORE THAT VALUE IN WORKING STORAGE
      CMA
      STA WS1
*LOAD INTO A THE BIT STRUCTURE OF THE
*HYBRID TRAY INPUT.
      STC HYBRG,C
      SFS HYBRG
      JMP *-1
      LIA HYBRG
      CLC HYBRG,C
      CLB
*ROTATE THE BIT STRUCTURE UNTIL THE DE-
*SIRED BIT IS IN POSITION 0.
TWIST ISZ WS1
      JMP *+2
      JMP CZECH
      RAR
      JMP TWIST
*TEST BIT 0 IN A, IF IT IS A 0 WRITE A 1
*IN B, IF IT IS 1 LEAVE B BLANK, AND
*TRANSFER B BACK TO THE FORTRAN PROGRAM
*AS JSTAT.
CZECH SLA,RSS
      INB
      ISZ SENSE
      LDA SENSE,I
      STB 0,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
```

```
*RETURN CONTROL TO THE FORTRAN CALLING
*PROGRAM.
       JMP WS4,I
       ENT ALCON
ALCON NOP
*TURN THE INTERRUPT SYSTEM OFF.
       CLF 0
*LOAD INTO A THE LAST WORD THAT WAS SENT
*TO THE HYBRID TRAY.
       LDA LSOUT
*BLANK OUT BITS 11-0 OF LSOUT AND WRITE
*IN THE HYBRID BIT STRUCTURE SPECIFIED
*BY JOUT.
       AND MSKHY
       LDB 0
       LDA ALCON,I
       STA WS4
*TRANSFER FROM THE FORTRAN PROGRAM THE
*BIT STRUCTURE TO BE DIRECTED TO THE
*HYBRID TRAY.
       ISZ ALCON
       LDA ALCON,I
       LDA 0,I
       AND MSKMO
       ADA 1
*OUTPUT A TO THE HYBRID REGISTER BUFFER.
       OTA HYBRG
*STORE THE UPDATED BIT STRUCTURE OF THE
*HYBRG OUTPUT WORD.
       STA LSOUT
*TURN THE INTERRUPT SYSTEM ON.
       STF 0
*RETURN CONTROL TO THE FORTRAN CALLING
*PROGRAM.
       JMP WS4,I
       ENT ALSEN
ALSEN NOP
*TURN THE INTERRUPT SYSTEM OFF.
       CLF 0
*LOAD INTO B THE HYBRID INPUT BIT
*STRUCTURE.
       STC HYBRG,C
       SFS HYBRG
       JMP *-1
       LIB HYBRG
       CLC HYBRG,C
*ALERT THE TTY TO EXPECT AN INPUT.
       LDA KNTRL
       JSB OUTPT
*COMPLEMENT B TO ACCOUNT FOR THE
*INVERSION IN THE HYBRID TRAY.
```

```
      CMB
*ROTATE BIT 11 OF THAT WORD TO THE 0
*POSITION IN THE REGISTER AND SEQUENT-
*IALLY READ THE 12 BITS AND OUTPUT THEIR
*VALUES (0 OR 1) TO THE TTY. ANS IS THE
*ASKII CODE OF 0, AND ANS+1 IS THE ASKII
*CODE FOR 1.
      BLF
      LDA MINI2
      STA WS1
RET   CLA
      RBL,SLB
      INA
      ADA ANS
      JSB OUTPT
      ISZ WS1
      JMP RET
*LOAD INTO A THE PACKED ASKII CODE FOR
*CARRIAGE RETURN LINE FEED, UNPACK THE
*CODE IN UNPAK AND OUTPUT THE CODE TO
*THE TTY.
      LDA CRLF
      JSB UNPAK
      LDA ALSEN,I
*TURN THE INTERRUPT SYSTEM ON.
      STF 0
*RETURN CONTROL TO THE FORTRAN CALLING
*PROGRAM.
      JMP 0,I
ADDSS DEF ONE
ONE   OCT 1
TWO   OCT 2
FOUR  OCT 4
TEN   OCT 10
SHOW  DEF AMPWO
AMPWO ASC 3,AMP #
POTWO ASC 3,POT #
ANS   OCT 260
BCD   BSS 1
BLKEQ ASC 1, =
CONVT DEF CONS1
CONS1 OCT 26
CONS2 OCT 62
CONS3 OCT 144
CRLF  OCT 6412
FIL7  OCT 200
FIL84 OCT 11
FIL01 OCT 40000
FIL10 OCT 100000
FIL11 OCT 140000
FIT01 OCT 10000
```

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FIT10  OCT 20000
FIT11  OCT 30000
FULL   DEF WORDS
WORDS  ASC 4,OVERFLOW
KNTRL  OCT 120000
LSOUT  OCT 0
MASK   OCT 377
MSK0   OCT 177776
MASKE  DEF MSK48
MSK48  OCT 37777
MSK30  OCT 147777
MSKMO  OCT 7777
MSKHY  OCT 170000
MSK4   OCT 17
MSK7   OCT 177
MSK82  OCT 177772
MSK84  OCT 177771
MINI2  OCT -14
MINUS  ASC 1,-
NEG3   OCT -3
NEG4   OCT -4
OWEPT  ASC 1,0.
PLUS   ASC 1,+
POS3   OCT 3
TEMPA  BSS 1
WS1    BSS 1
WS2    BSS 1
WS3    BSS 1
WS4    BSS 1
       END
```

IX. REVISIONS TO MANUALS

The following changes have been made to one set of manuals available in the Hybrid Computer Center.

Changes to EAI TR-48 Analog Computer Reference Handbook[23].

P1-15 at the end of the first paragraph, write ", with the exception of the hybrid mode, in which case a bottle plug must be used to connect the DVM input line to the SEL termination."

P1-20 Section 1.3.6, after the last sentence insert the following sentence: "When the ANALOG/HYBRID master switch is in the HYBRID position, these pushbuttons are disabled (all lamps are extinquished) and the TR-48 is automatically slaved to the DES-30. The HD, PS, IC, OP, and RO modes are controlled by the DES-30 or by the digital computer through the DES-30 when in the HYBRID Mode."

P 2-1 Section 2.1.2 - At the end of sentence three, following "SELECTOR switch", insert "or Hybrid automatic addressing system".

Changes to EAI DES-30 Digital Expansion System Reference Reference Series[24].

P 1-2, number 5 Clocking - in the first sentence after "AND gates", insert the words "the Hybrid Sense and Control lines, and the OP and RST Inputs,".

P 1-7, Section 10.1 under "DES-30 Mode" in the table, change the following: add to the first sentence after the

words "control pushbuttons," the words "or digital computer"; delete the last sentence "Not allowed" and insert in that place the words "RUN, and TR-48 TIME SCALE FAST."

P 1-9, Section 11.1 - In the table under "TR-48 mode", delete "Not Allowed" and replace it with "Pot Set". Under "Note" after "SL", insert "or Hybrid."

P 1-10, Section 11.3. Insert after the words "(Figure 2)" the words "or by the digital computer, or by the presence of logical ones at the RUN and CLR DES-30 inputs,".

P 1-15 - Insert a new section,

"12. HYBRID DES-30/2116B Digital Computer Interface

12.1 Control Lines - control lines numbered 0 to 11 are provided on the HYBRID Trunk Tray. These lines are set to a logical zero or logical one state by the digital computer software (See Hybrid System User's Manual).

12.2 Sense Lines - Sense lines numbered 0 to 11 are provided on the Hybrid Trunk Tray. The logical states of these lines may be tested by the digital computer software (See Hybrid System User's Manual).

12.3 DES-30 and TR-48 Mode Control - Digital Control of the DES-30 and TR-48 from the 2116B digital computer is provided through the Hybrid System Executive Software (See Hybrid System User's Manual).

Changes to EAI TR-48 Analog Computer EMC Model 45-117 Maintenance Manual Volume 1[25]

P 1-9, Section 1.5.3, Paragraph 2 - at the end of the sentence add ", unless the Hybrid Mode has been selected by placing the ANALOG/HYBRID switch into the HYBRID position, which automatically slaves the computers."

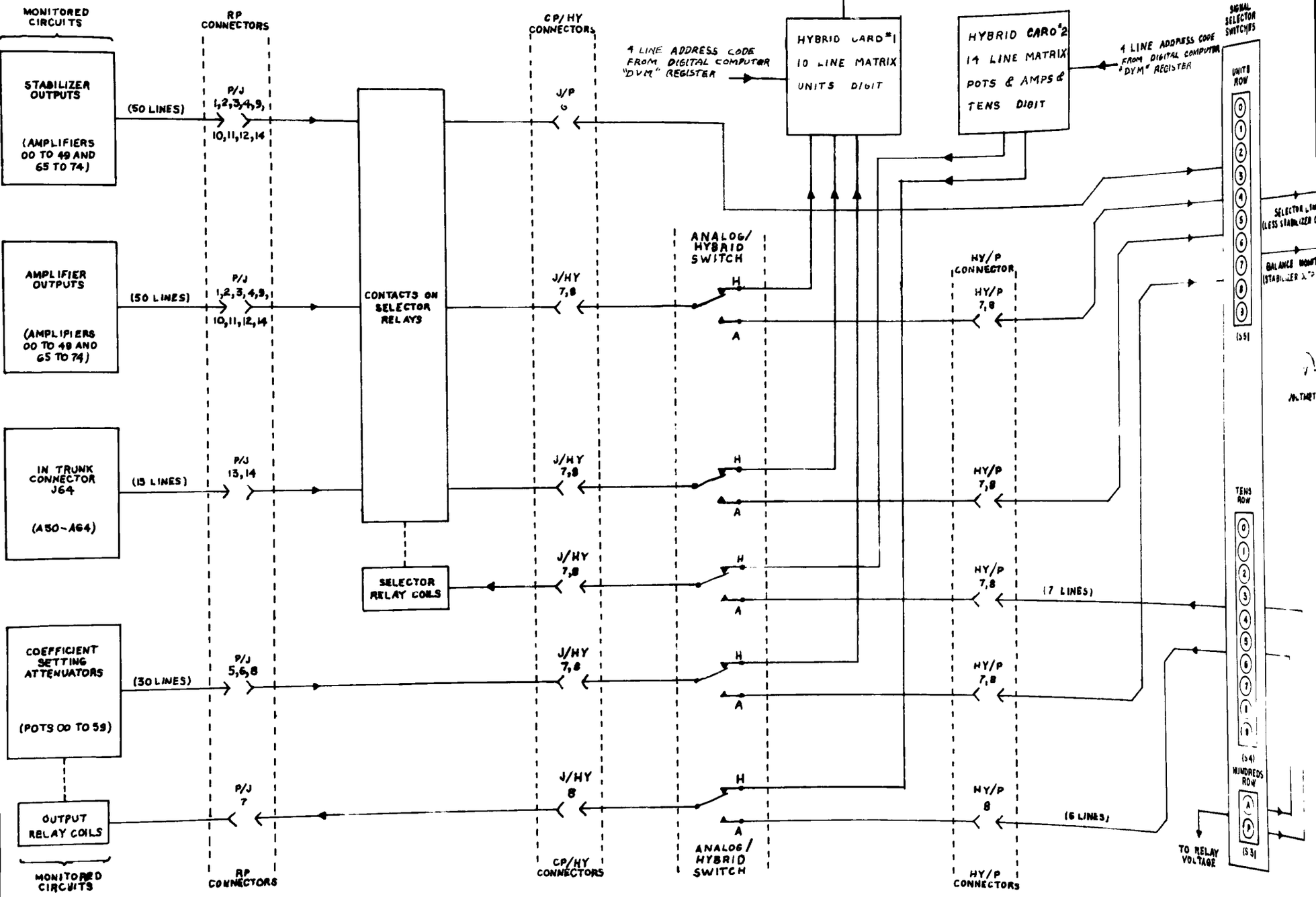
P 1.14, Section 1.6.3 - insert after the last sentence: "with the exception of the hybrid mode in which case a bottle plug must be used to connect the DVM input line to the SEL termination."

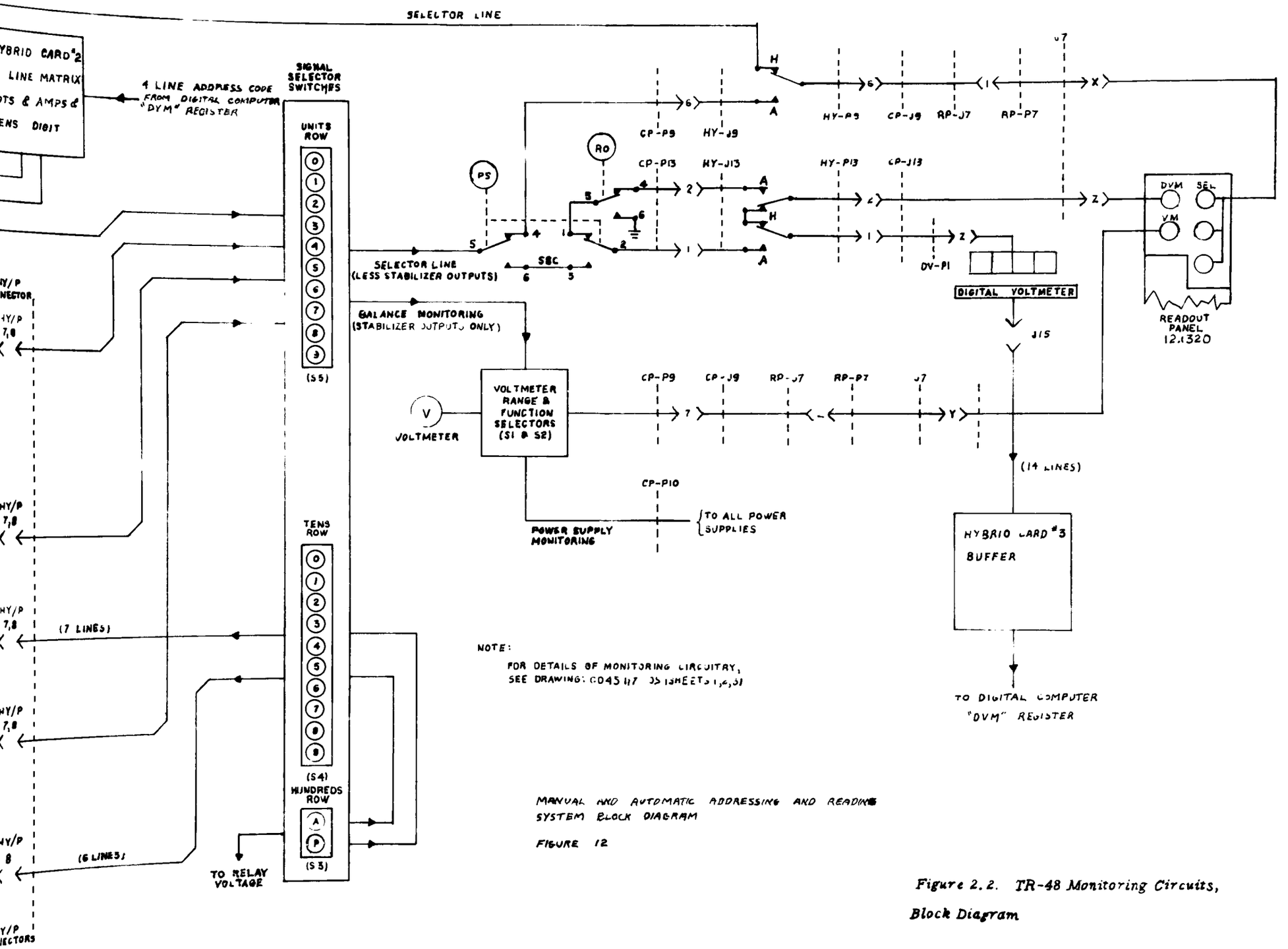
P 1.14, Section 1.6.4 - Insert after the first paragraph: "ANALOG/HYBRID Master Switch - when the ANALOG/HYBRID Master Switch is in the HYBRID position, the mode pushbuttons are disabled (all lamps extinquished) and the TR-48 is automatically slaved to the DES-30 and digital computer. The HD, PS, IC, OP and RO modes are controlled through the DES-30 when in the HYBRID mode. When the switch is in the ANALOG position, the TR-48 is free to be controlled manually by the mode push-buttons, and may operate as a separate system."

P 1.18 Place an asterisk (*) after "pot-set mode" in #1 of both sets of instructions. Place a footnote at the bottom of the page: "*Note: For the purpose of patch panel insertion or removal, the pot-set mode must be selected by the mode pushbuttons when the ANALOG/HYBRID master switch is in the ANALOG position."

P 2.3 - Replace Figure 2.2 with Figure 12.

P 2.4 - At the end of the first paragraph add "with the exception of the Hybrid Mode, in which case the bottle plug


MONITORED CIRCUITS
RP CONNECTORS
CP/HY CONNECTORS
4 LINE ADDRESS CODE FROM DIGITAL COMPUTER "DVM" REGISTER
HYBRID CARD #1
10 LINE MATRIX
UNITS DIGIT
HYBRID CARD #2
14 LINE MATRIX
POTS & AMPS &
TENS DIGIT
4 LINE ADDRESS CODE FROM DIGITAL COMPUTER "DVM" REGISTER
SIGNAL SELECTOR SWITCHES
UNITS ROW
STABILIZER OUTPUTS
(AMPLIFIERS 00 TO 49 AND 65 TO 74)
(50 LINES)
P/J 1,2,3,4,9, 10,11,12,14
J/P 6
AMPLIFIER OUTPUTS
(AMPLIFIERS 00 TO 49 AND 65 TO 74)
(50 LINES)
P/J 1,2,3,4,9, 10,11,12,14
CONTACTS ON SELECTOR RELAYS
J/HY 7,8
ANALOG/ HYBRID SWITCH
H
A
HY/P CONNECTOR
HY/P 7,8
(55)
IN TRUNK CONNECTOR J64
(A50-A64)
(15 LINES)
P/J 13,14
J/HY 7,8
HY/P 7,8
TENS ROW
SELECTOR RELAY COILS
(7 LINES)
COEFFICIENT SETTING ATTENUATORS
(POTS 00 TO 59)
(30 LINES)
P/J 5,6,8
J/HY 7,8
HY/P 7,8
(54)
HUNDREDS ROW
OUTPUT RELAY COILS
P/J 7
J/HY 8
HY/P 8
(6 LINES)
TO RELAY VOLTAGE
(53)
MONITORED CIRCUITS
RP CONNECTORS
CP/HY CONNECTORS
ANALOG/ HYBRID SWITCH
HY/P CONNECTORS



NOTE:

FOR DETAILS OF MONITORING CIRCUITRY, SEE DRAWING: CD45117 JS13SHEETS 1,6,51

MANUAL AND AUTOMATIC ADDRESSING AND READING SYSTEM BLOCK DIAGRAM

FIGURE 12

Figure 2.2. TR-48 Monitoring Circuits, Block Diagram

must be used to connect the SEL to the DVM termination."

P 2.5, Section 2.1.3.2 - In the last sentence of the first paragraph between "...HD/SL (hold/slave) switch depressed," and "the computer can only...," insert the phrase "or the ANALOG/HYBRID Master Switch in the Hybrid position,".

Section 2.2 at the end of the third sentence insert ", or the Hybrid Mode is selected."

P 2.6, Table 2.1 - Under "mode" and beneath "Slave (SL)", write "HYBRID".

P 12.3, Section 12.2.1 - Insert after the first sentence of paragraph 2 the following: ", or by calling the Hybrid system executive software to automatically address and read-out the value of the pot when in the HYBRID mode."

Changes to EAI TR-48 Analog Computer EMC Model 45.117 Maintenance Manual Volume 2[26].

Drawing D 045 117 OS Schematic EMC computer sheets 1,2,3 incorporate the ANALOG/HYBRID Master Switch from Table 8 and figure 4, subsystem Interconnection Diagram.

Drawing B 093 033 OW, Sheet #40, J61 - J62 - For J61-3, insert "Mode Control enable - A/H switch Term 26.

Changes to EAI DES-30 Digital Expansion System Maintenance Series[27].

1. P 1-12, Figure 7 - Delete lines B and C from connector A15-J2.
2. Drawing D093021 OW Sheet 3 - Under (15) Digital I/O at A15J1, change "D-I" to "D-O" and at A15J2, change "D-O" to "D-I".

Add a wire from A27J1-E to A15J1-D.

Delete the wires from A27J1W,V,S and T to J47 v,r,DD and Z.

Add wires from A27J1-S and T to A15J1 R and L.

Add wires from A15J1-W and X to J47 v and r.

Delete the wire from A27-J2S to J47 CC.

Add a wire from A27J2 S to A1 -J2 X.

Add a wire from A15-J1Y to J47CC.

Add a wire from J47 Z to A15J2 Z.

Add a wire from J47 DD to A15-J1 Z.

Delete the wire from A15-J2 A,B,C to buses.

Add a wire from A15-J1 A to J45 pin BB.

Add wires from A15-J2 pins A B C and E to J45 Pins B FF H HH.

3. Drawing D063 173 OS
Schematic Slave Tray (EMC) following P34-7

On A1

Reset (In) #4 delete the wire from the 10K resistor to input #1 of 8d, and the wire going from CR7 to A27 P1 pin V, then add a wire going from the 10K resistor to A27 P1 pin V.

Operate (In) #3 - delete the wire from the 10K resistor to input #5 of 8d and the wire going from CR9 to A27P1 pin W, then add a wire going from the 10K resistor to A27P1 pin W.

On A2

Run In #5 - delete the wire going from the 10K resistor to input #5 on 7C. Add a wire going from the 10K resistor to A27-P1 pin R. Add a wire from A27-P1

pin T to input #5 on 7C.

CLR In #6 - delete the wire going from the 10K resistor to input #1 on 7C. Add a wire going from the 10K resistor to A27P1 pin P. Add a wire going from A27P1 pin S to input #1 on 7C.

4. P44-3, Figure 3

In the DES-30 portion, change the nomenclature on the left most connector to read J47 instead of A27J1. Delete the Time Scale, RST, and OP cables. Add Time Scale, RST, OP, POT SET, AND ENABLE Cables from A15J1 Y,X,W,Z and A15J2 Z to J47 CC,r,v,DD and Z.

In the TR-48

Delete J61-3 to J7A-A

Add J61-4 Pot Set to CP J13-11 and J61-3 ENABLE to ANALOG/HYBRID Switch Terminal 26H.

X. TESTING AND OPERATING PARAMETERS

A FORTRAN program was written to aid in the debugging of the interface system. The program tested the entire system. Errors in typing and drawings in the manuals, and interpretive errors led to many changes during testing. Also as a result of testing many design modifications were made in hardware and software to improve system performance and reliability.

First the testing of the TR-48 and DES-30 mode control was done in the ANALOG mode using the DES-30 patch panel, then in the HYBRID mode by calling the modes from the 2116B and checking the buses on the rear of the TR-48 and DES-30 with an oscilloscope to see that they had switched. The times for initiating the modes from the FORTRAN Program were measured. The results are as follows:

Mode	Time in Microseconds
Operate	33
Reset	32
Pot Set	350
Hold	31
Stop	31
Clear	34
Run	33
Time Scale Fast	33

Mode Controlling Times - The interval between the time of initiation of the FORTRAN CALL statement and the time the bus switches.

Table 10

As there was no requirement for high speed switching in the Pot Set mode a relay was used in the design to facilitate voltage conversion. This increased the switching time for the Pot Set mode. All other modes incorporate electronic switches.

Next the modes were tested from the DES-30 slave tray patch block to see that the mode control hierarchy worked. The time required to switch the TR-48 from OP to RESET was approximately .8 microseconds using the mode control hierarchy.

Next the Pot and Amplifier Addressing and Reading System was tested by having the software print the values of all pots and amps onto the teletype. The pots and amps were selected manually and then read out on the DVM readout panel and recorded. The values read manually corresponded exactly to those read out automatically, with the exception, of course, that the values readout automatically were truncated by one digit.

Next, the pots and amps were read in rapid succession automatically in a DO loop in the FORTRAN program. The time required to address and read all 45 pots was 90 seconds and all 75 amps was 150 seconds.

The control lines were all tested individually by reading the line number and state from the teletype and calling the line from the FORTRAN routine CONT and patching its output on the DES-30 to a register indicator lamp. The time from the FORTRAN call statement to the time the first control line switches on the DES-30 patch panel was measured on an

oscilloscope to be 180 microseconds; add 20 microseconds for each successive control line.

The sense lines were tested individually using the SENSE routine by reading the line number from the TTY, then printing onto the TTY the state of that line. The time from the call of the first sense line in the FORTRAN program to the time the state of that sense line is returned to the FORTRAN calling routine was calculated to be approximately 57.2 microseconds; add 8.4 microseconds for each successive sense line. This was calculated since there was no way of determining experimentally exactly when the FORTRAN program was re-entered.

A number of bit configurations for the control lines were tested using the ALCON hybrid system routine. The bit structure was read in from the teletype, control lines were patched to their respective sense lines, and the bit structure was typed out using the ALSEN Routine.

Finally, the ANALOG/HYBRID switch was turned to ANALOG and the systems; i.e., the automatic and manual mode control and addressing, were checked to see that they were truly demated.

XI. RECOMMENDATIONS

This section contains recommendations for further additions and modifications to the TR-48, 2116B, DES-30 and interface system.

1. A color code should be adopted to designate the Hybrid System. An indicator light of the Hybrid color could be mounted next to the ANALOG/HYBRID master switch on the TR-48 and would be powered through the master switch to light when the system is in the HYBRID mode. Indicator lights could be added to the DES-30 and 2116B panels in a similar fashion. All components of the interface could be painted this color for easy identification.

2. The controls on the TR-48 which are inhibited in the HYBRID mode could be stenciled in a cluster as a reminder that they are inhibited. These controls include the Selector push-buttons, the Mode control pushbuttons, the Patch Panel ENGAGE/DISENGAGE switch and the Rep Op Compute Time Vernier.

3. A power switch should be added to the front panel of the HP3030 Magnetic System so that after the compiled hybrid program and associated library routines are loaded into the 2116B core, the tape may be dismounted and the Magnetic Tape System easily turned off if the system is not needed during the hybrid operation.

4. A relay system could be added between the SEL and the DVM terminals that would be called from the software program. This would make the use of the bottle plug shorting bar

unnecessary. When pots or amps are being read in the pot set or reset mode, the shorting bar would effectively be put into place by the software and relay system. If the relay system detaches the SEL and DVM terminals from the patch panel, an amplifier or other component could be pre-patched to the DVM outlet without affecting the reading of the pots and amps. The relay system could also deactivate the plotter and ground the DVM automatically when the software is in the Rep Op mode as the manual system does.

5. The mode control pushbutton lamps are all extinguished in the Hybrid mode. It would be convenient to know by indicator lamp to what mode the 2116B or DES-30 has controlled the TR-48. The mode indicator lamps could be keyed to the operate, reset and pot set buses in the rear of the TR-48. The INT (internal) indicator would never be lit and the HD/SL (hold/slave) indicator would always be lit in the HYBRID mode. Some means of inhibiting the OP and RS indicators and illuminating the RO indicator during the rep op mode would be required to keep the OP and RS lamps from alternately flashing as those modes are switched during the rep op mode. Another control line and software from the 2116B and logic in the TR-48 would probably be required from the Rep Op indicator. Neither the manufacturer of the DES-30 nor the designer of this interface system take into account the tracking of the DES-30 mode with the logical inputs to the RUN, CLR terminations on the patch panel; that is, the RUN mode indicator is always lit

when the DES-30 is controlled by logic level of the DES-30 or 2116B no matter what mode is selected. The lamps could be wired to coincide with the modes of the DES-30.

6. Additional Control and Sense line capability may be added by purchasing another HP+16 duplex register and another EAI Tray for the DES-30 and wiring the system as the present Hybrid I/O tray is wired. The hybrid system software routines, CONT, SENSE, ALCON AND ALSEN, would change only in the select code address of the register. Additional control and sense line capability could also be gained with the present HP registers by utilizing the six unused read and nine unused write bits from the Hybrid and DVM registers, and by Utilizing any unused bits from other registers currently in the 2116B.

7. A hybrid system subroutine could be added to read the pots when the TR-48 is in any mode instead of the pot set mode only as this interface system provides. A subroutine could also be added to read the amplifiers when the TR-48 is in any mode instead of the reset mode only as this interface system provides.

8. A more flexible means of calling the REPOP mode could be made by additional software. For example, a FORTRAN callable time could be included to provide increments between 20 and 200 milliseconds by recycling the HP crystal clock for varying times. The time would be transferred from the FORTRAN program to an assembler timer program by a FORTRAN

statement like CALL REPOP (ITIME).

9. The DES-30 or TR-48 is capable of controlling the TR-48 modes very quickly as a result of the software by using the DES-30 hierarchy capability as explained previously. The sense and control lines provide means of sampling a point on the TR-48 and DES-30 and initiating a logical control relatively slowly as the result of the software. However, a faster means of sampling a point and initiating control as a result of software can be provided by the use of interrupt lines. These lines would be wired from the DES-30 or TR-48 patch panel to the Flag bits of the Hybrid or DVM registers in the 2116B. If during the running of a program on the 2116B (with the 2116B interrupt system turned on) a flag bit were to be set by one of these interrupt lines, control of the program would be transferred during the interrupt portion of the 2116B machine cycle indirectly through the core location equivalent to the select code of the interrupting register to the location in which the controlling subprogram is stored. Higher speed lines could also be achieved using Durect Memory Access (DMA).

10. As an aide in set up of a problem, the software could be programmed to sequentially address the pots to be set, thereby eliminating manual addressing. This could be accomplished by altering the Hybrid System Executive Software Program AMPOT to wait for a specified length of time after 'POT#__=' is printed out. A better method would be to put a

pushbutton on the TR-48 attenuator panel hooked to the DVM register flag bit. In this manner, the user would specify perhaps in a DO loop the pots that he wants to set. The first pot number would be called in the FORTRAN routine, transferred to the pot reading routine where the pot would be addressed and 'POT#__=' would be printed onto the teletype. The user would set the pot by the DVM readout then push the button to the flag signalling the software to proceed and type out the pot value on the teletype for permanent record. The FORTRAN program would then step to the next pot to be read.

11. A software program for storing pot values and static amplifier values on magnetic tape could be devised using the pot and amp addressing and reading system. These values could be printed out onto the teletype prior to the next running of the program to aid in pot setting and static checks.

12. Computer programs can be written to aid in the set-up of time scaling, magnitude scaling and coefficient determination.

13. As discussed in SYSTEMS CONCEPTS, the four BCD lines representing the DVM least significant bit were dropped. A way of regaining this LSB for no loss of information would be to use the 4 vacant read bits on the Hybrid register. This would mean changing the logic level of the DVM output, logical zero = +2 volts and a logical one = -12 volts, to that of the Hybrid register where a logical zero = +12 volts and a

logical one = 0 volts. A change in the Hybrid System Executive Software would also have to be made to account for reading the bits, decoding them, and writing the LSB onto the teletype. Another method of reading the LSB would be to use the remaining 2 bits and the flag bit in the DVM register. The 1's bit could be dropped and the 2's, 4's, and 8's bits could be sent to the 2116B with a loss of accuracy of only .0001 machine units. Another method would be to use the LSB to determine whether or not the 4th MSB should be rounded-off. This could be accomplished by one more bit to the DVM register. The output of an OR gate with the 1 and 2 LSB inputs would be AND'ed with the 4 input. The output of this gate would be OR'ed with the 8's bit. The output of this gate would be a zero if the LSB is less than 5 or a one if the LSB is greater than or equal to 5.

14. During the course of this thesis a new solid state coded line selector module has become available from some of the semiconductor manufacturers. With some voltage level buffers and inverters the selector modules could be used in lieu of the diode matrices used in this project for the addressing system. These modules would be easier to assemble and easier to service than the diode matrices.

15. Frequently used software routines making reference to the Hybrid System Executive Software could be added to the library tape. These would be routines such as a REPOP or POT and AMP sequencing routines which control and call

the Hybrid System Executive Software Routines. The main advantage to these routines would be saving repetious programming and saving core since they would not be loaded into memory unless they were called.

16. The DES-30 OP and RST outputs are provided from the output of the parallel mode control logic, open loop, in a similar fashion to that of the manufacturer's original equipment. A more meaningful output at these points could be achieved by sampling the OP and RST busses at the rear of the TR-48, closed loop, and returning the signals to the DES-30 to verify the mode of the TR-48.

17. The plotter operate and reset is not available when the TR-48 is in the slave mode as a result of the manufacturer's original equipment. With some wiring changes in the TR-48 this could be provided.

18. This thesis provides entry from a FORTRAN program to the Hybrid System Executive Software written in ASSEMBLER. Entry to the Hybrid System Executive Software from BASIC should also be investigated.

XII. EXTENT TO WHICH OBJECTIVES WERE ACCOMPLISHED

A system has been built to perform all of the originally required tasks. The system operates as required, as evidenced by the section on Testing and Operating Parameters.

A great deal of flexibility has been maintained in this system, both in the operation and in the capability for additions and modifications.

Both the hardware and software interfaces with the user have been human factored for ease in system usage.

Care has been taken to use reliable hardware and still stay within the economic limits of this project. However, the overall system reliability will become evident only after the system has performed for some time.

This project perhaps did not thoroughly maintain simplicity, but it is felt that using as much as possible the systems that were present in the machines to perform the required tasks rendered this a much simpler system than would have otherwise been possible.

Total modularity was nearly achieved. The systems in the 2116B and the TR-48 are all modular, plug-in devices. The Hybrid I/O tray constructed for this project for insertion into the DES-30 is modular. The only changes that were made that were not of a modular fashion were minor changes to the DES-30 Slave Tray, minor changes to the DES-30 back-plane wiring, and two wire routings in the TR-48. Whenever possible the system was designed to include existing wiring; this was

accomplished in most instances.

It is conceivable that this interface system could be utilized in linking a TR-48 and DES-30 to nearly any 16-bit (or greater) digital computer with very minor alterations required only if different voltage levels are employed. Advantages of using this linkage system for other computers are its extremely low cost, flexibility, and near modularity. The software obviously may require considerable renovation depending upon the digital computer and its peripheral devices.

It was hoped at the beginning of this thesis that the amount of core required by the Hybrid system executive software could be held to less than 1K. The final Hybrid System Executive Software requires 423 locations in memory.

Because most of the hardware was designed to incorporate components that were in stock at RIT, many of them industrial gifts, final cost of the system does not accurately reflect what the total system costs would have been had there been no stock available. Components used from stock included resistors, transistors, wiring, diodes, logic boards and mounting hardware. Components that were purchased included relays, connectors and pins, a switch, and a tray and panel blocks for the DES-30.

The total expenditure for the purchased equipment was $234.61. This is well below the original estimate of $400 to $1000. The estimated expenditure for stocked equipment was $400.

XIII. CONCLUSIONS

As our world becomes more complex, the requirement to simulate total systems will inevitably increase. The hybrid computer is fast becoming one of the accepted tools for solving total systems problems. It is anticipated that as a result of this thesis, the Rochester Institute of Technology students and faculty will be better able to contribute to the solution of man's problems through education and technology.

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